Search Results 09/470,542

L Number	Hits	Search Text	DB	Time stamp
1	739	326/30.ccls.	USPAT; US-PGPUB	2001/11/28 10:51
4	698	710/100.ccls.	USPAT; US-PGPUB	2001/11/28 10:52
7	16	326/30.ccls. and 710/100.ccls.	USPAT; US-PGPUB	2001/11/28 11:00
10	213545	resistor$1	USPAT; US-PGPUB	2001/11/28 11:44
13	26251	25$ with 65$	USPAT; US-PGPUB	2001/11/28 11:14
14	0	("25" adj ohms) near5 ("65" adj ohms)	USPAT; US-PGPUB	2001/11/28 11:15
17	2	("25" adj2 ohms) near5 ("65" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:20
20	0	("25" adj2 ohms) near5 ("65" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:20
25	0	("25" adj3 ohms) near10 ("65" adj3 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:20
30	6	("25" adj3 ohms) near10 ("65" adj3 ohms)	USPAT; US-PGPUB	2001/11/28 11:22
33	365	resistor$1 same (25$ with 65$)	USPAT; US-PGPUB	2001/11/28 11:22
36	0	(326/30.ccls. and 710/100.ccls.) and (resistor$1 same (25$ with 65$))	USPAT; US-PGPUB	2001/11/28 11:23
39	16	(326/30.ccls. and 710/100.ccls.) and 326/30.ccls.	USPAT; US-PGPUB	2001/11/28 11:23
42	1	(resistor$1 same (25$ with 65$)) and 326/30.ccls.	USPAT; US-PGPUB	2001/11/28 11:24
45	1	(resistor$1 same (25$ with 65$)) and "2"	USPAT; US-PGPUB	2001/11/28 11:24
48	0	(resistor$1 same (25$ with 65$)) and 710/100.ccls.	USPAT; US-PGPUB	2001/11/28 11:24
51	50119	terminat$ with (line$1 or bus or buses or busses)	USPAT; US-PGPUB	2001/11/28 11:44
54	16	(326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))	USPAT; US-PGPUB	2001/11/28 11:30
57	16	((326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))) and resistor$1	USPAT; US-PGPUB	2001/11/28 11:33
60	763	"about" near5 ("50" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:45
63	0	(((326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))) and resistor$1) and ("about" near5 ("50" adj2 ohms))	USPAT; US-PGPUB	2001/11/28 11:37
66	26	(terminat$ with (line$1 or bus or buses or busses)) same ("about" near5 ("50" adj2 ohms))	USPAT; US-PGPUB	2001/11/28 11:37
69	9	resistor$1 same ((terminat$ with (line$1 or bus or buses or busses)) same ("about" near5 ("50" adj2 ohms)))	USPAT; US-PGPUB	2001/11/28 11:37
72	14069	terminat$ with (line$1 or bus or buses or busses)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
77	246378	resistor$1	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
82	21	"about" near5 ("50" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
87	0	(terminat$ with (line$1 or bus or buses or busses)) same resistor$1 same ("about" near5 ("50" adj2 ohms))	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:46
92	1246	(terminat$ with (line$1 or bus or buses or busses)) same resistor$1	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:46

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97	11	(terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:58
102	283	(terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:59
105	570	"7" adj3 "12" adj3 (percent or "%")	USPAT; US-PGPUB	2001/11/28 12:01
108	0	((terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)) same ("7" adj3 "12" adj3 (percent or "%"))	USPAT; US-PGPUB	2001/11/28 12:01
111	0	((terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)) and ("7" adj3 "12" adj3 (percent or "%"))	USPAT; US-PGPUB	2001/11/28 12:02
114	2	percent$ same ((terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms))	USPAT; US-PGPUB	2001/11/28 13:24
117	1	6067594.uref.	USPAT; US-PGPUB	2001/11/28 13:26
120	0	6067594.ref.	USPAT; US-PGPUB	2001/11/28 13:28
123	1	6067594.pn.	USPAT; US-PGPUB	2001/11/28 13:46
126	1		USPAT	2001/11/28 13:29
127	1		USPAT	2001/11/28 13:29
128	1		USPAT	2001/11/28 13:30
129	1		USPAT	2001/11/28 13:30
130	1		USPAT	2001/11/28 13:30
131	1		USPAT	2001/11/28 13:31
132	1		USPAT	2001/11/28 13:31
133	1		USPAT	2001/11/28 13:31
134	1		USPAT	2001/11/28 13:32
135	1		USPAT	2001/11/28 13:32
136	1		USPAT	2001/11/28 13:33
137	1		USPAT	2001/11/28 13:33
138	1		USPAT	2001/11/28 13:33
139	1		USPAT	2001/11/28 13:33
140	1		USPAT	2001/11/28 13:34
141	1		USPAT	2001/11/28 13:34
142	1		USPAT	2001/11/28 13:34
143	1		USPAT	2001/11/28 13:42
144	1		USPAT	2001/11/28 13:42
145	1		USPAT	2001/11/28 13:43
146	139	rambus.asn.	USPAT; US-PGPUB	2001/11/28 13:47
149	58	(terminat$ with (line$1 or bus or buses or busses)) and rambus.asn.	USPAT; US-PGPUB	2001/11/28 14:38
152	3327	terminat$ with (both adj2 end$1)	USPAT; US-PGPUB	2001/11/28 14:40

155	495	(terminat$ with (line$1 or bus or buses or busses)) same (terminat$ with (both adj2 end$1))	USPAT; US-PGPUB	2001/11/28 14:42
158	12152	710/$.ccls.	USPAT; US-PGPUB	2001/11/28 14:42
161	10528	326/$.ccls.	USPAT; US-PGPUB	2001/11/28 14:42
164	14	326/$.ccls. and 710/$.ccls. and ((terminat$ with (line$1 or bus or buses or busses)) same (terminat$ with (both adj2 end$1)))	USPAT; US-PGPUB	2001/11/28 14:43

US-CL-CURRENT: **326/30,710/100**

US-PAT-NO: 6078978
DOCUMENT-IDENTIFIER: US 6078978 A
TITLE: Bus interface circuit in a semiconductor memory device
DATE-ISSUED: June 20, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Suh; Jung Won	Kyungki-do	N/A	N/A	KRX

US-CL-CURRENT: **710/305,326/30 ,710/100**

ABSTRACT:
This invention relates to a bus interface circuit in a semiconductor memory device. This invention comprises a data driver to transmit a data signal through a first transmission line of which one end is terminated; a reference voltage driver to transmit a reference voltage signal through a second transmission line of which one end is terminated; and a receiver to determine a logic state by comparing the data signal transmitted by the first transmission line with the reference voltage signal transmitted by the second transmission line. Accordingly, a high-speed bus interface circuit of the present invention can decrease a common mode noise, influence of ground bounce, an output voltage swing and a power consumption by simultaneously driving a data driver and a reference voltage driver in a memory interface using a transmission line being either single or parallel terminated to transmit to a receiver.
5 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

BSPR:
In drawings attached to this specification, reference Rt shows a termination resistor. The **termination** resistor is matched with specific impedance of a transmission **line** and prevents reflection of a transmitted signal, thereby preventing distortion of signals. References R1 and R2 show resistors to generate a reference voltage Vref in a conventional bus interface. The resistors R1 and R2 generate the reference voltage Vref from a board by a resistance rate, in which the reference voltage is commonly used in a receiver of each chip. Single **termination** means that one end of the **termination line is terminated**; while parallel **termination means that both ends of the termination line are terminated**. The receiver concludes logic 1 or logic 0 by comparing a data signal transmitted to the transmission line with the reference voltage Vref. A driver is an open drain structure. The logic 1 or logic 0 is transmitted to the receiver through the transmission line by turning off or turning on a NMOS driver (See description of FIGS. 2 to 5).

BSPR:
A high-speed **bus** interface circuit comprises of a data driver to transmit a data signal through a first transmission **line of which both ends are terminated**; a reference voltage driver to transmit a reference voltage signal through a second transmission **line of which both ends are terminated**; and a receiver to determine a logic state by comparing the data signal transmitted by the first transmission **line** with the reference voltage signal transmitted by

the second transmission **line**.

BSPR:
A high-speed **bus** interface circuit comprises of the first chip having N data driver to transmit N data signals through transmission **lines of which both ends are terminated** and M reference voltage driver to transmit a reference voltage signal through a transmission **line of which both ends are terminated** and N receiver to determine a logic state by comparing the data signals transmitted by the transmission **lines** with the reference voltage signal transmitted by the transmission **line**; a second chip having N data driver to transmit N data signals through transmission **lines of which both ends are terminated** and M reference voltage driver to transmit a reference voltage signal through a transmission **line of which both ends are terminated** and N receiver determines the logic state by comparing the data signals transmitted by the transmission **lines** with the reference voltage signal transmitted by the transmission **line**; a plurality of transmission **lines of which both end are terminated** to transmit N data signals between the first chip and the second chip; and a plurality of transmission **lines of which both ends are terminated** to transmit M reference voltage signals between the first chip and the second chip.

DEPR:
As described above, the reference voltage signal Vref and the data signal are transmitted to the receiver 33 through the transmission line having identical environment. If the transmission line for the data signal and the transmission line for the reference voltage signal are arranged as in FIG. 4, the common mode noise affecting to the transmission lines can be reduced. When a driving condition of the data driver 31 is changed due to the ground bounce, the driving condition of the reference voltage driver 32 is also changed as described in FIG. 2A. Accordingly, influence of the ground bounce can be decreased. When the transmission **line** is parallel **terminated,** signal reflection from **both ends** of the transmission **line** can be prevented and signal distortion is decreased compared to the single **termination**. However, the driving current of the data driver 31 and the reference voltage driver 32 is increased, whereby power consumption is increased.

CLPV:
a data driver to transmit a data signal through a first transmission **line of which both ends are terminated**;

CLPV:
a reference voltage driver to transmit a reference voltage signal through a second transmission **line of which both ends are terminated**; and

CCOR:
710/305

CCXR:
326/30

CCXR:
710/100

US-CL-CURRENT: **326/30**,370/402 ,**710/100**

US-PAT-NO: 6067596
DOCUMENT-IDENTIFIER: US 6067596 A
TITLE: Flexible placement of GTL end points using double termination points
DATE-ISSUED: May 23, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nguyen; Thu Q.	Tomball	TX	N/A	N/A
Phu; Hung Q.	Friendswood	TX	N/A	N/A

US-CL-CURRENT: **710/306**,**326/30** ,370/402 ,**710/100**
ABSTRACT:

A highly parallel computer system including dual processors and dual memory controllers are coupled to an Assisted Gunning Transceiver Logic Plus (AGTL+) high speed system bus. The microprocessors are designed for a quad processor architecture requiring four processors and four connectors for the processors. To maintain signal timing and integrity in a dual processor/dual memory controller architecture, additional terminations are inserted. Printed circuit
board space is conserved with a dual processor architecture. The additional connectors and traces to the additional connectors for the processors are no longer needed. Furthermore, with the dual processor design, there is no need for two additional termination cards.
20 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

DEPR:
AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic and termination. AGTL+ buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to "assist" the pull-up resistors
during the first clock of a low-to-high voltage transition. As has been discussed, in order to achieve that desired high performance and to assure signal integrity, Intel has imposed strict electrical and mechanical constraints or guidelines for a computer system implementing the XEON host bus.
(See e.g., Intel Application Note AP-830, Pentium II XEON Processor/Intel 450NX
PCIset AGTL+ Layout Guidelines, herein incorporated by reference). These guidelines include limitations on bus trace length, trace topology, and device positioning. In particular, the XEON host bus standard specifies a maximum of six XEON host bus loads. Also, XEON host bus processors must reside on the electrical ends of the bus. In addition, the XEON host **bus** is required to be electrically **terminated at both ends,** and XEON host **bus** devices are required to
be evenly spaced along the XEON host **bus**. Furthermore, the XEON processor is designed for use in a quad processor system. For use in a dual processor architecture, Intel recommends insertion of terminations in lieu of the other two processors. These are only a few of the specified guidelines. As can be seen, they are significant constraints on design.

CCOR:
710/306

CCXR:

326/30

CCXR:
710/100

US-CL-CURRENT: **326/30**,375/211

US-PAT-NO: 5961619
DOCUMENT-IDENTIFIER: US 5961619 A
TITLE: Method and apparatus for automatic activation of bus termination on a fast ethernet repeater stack
DATE-ISSUED: October 5, 1999
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Voloshin; Moshe	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: **710/300**,**326/30** ,375/211
ABSTRACT:

An automatically activated bus termination circuit in a repeater which is suitable for inclusion in a repeater stack including an end unit determination circuit. The end unit determination circuit includes a local input connector having an input sense pin. The input sense pin is configured to be connected to an input sense potential when the local input connector is connected to a remote output connector having an output sense pin. The output sense pin is configured to be connected to an output sense potential when the local output connector is connected to a remote input connector. The bus termination circuit is configured to be active when either the input sense pin is not connected to the input sense potential or the output sense pin is not connected
to the output sense potential. As a result, the bus termination circuit is activated when a stack bus connection cable is not connected from the local output connector to a remote input connector or when a stack bus connection cable is not connected from the local input connector to a remote output connector.

20 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

DEPR:
It is important that the **termination** circuit be activated even when one or **both**
of the end units is powered off. Otherwise, a powered off end unit would not be **terminated** and would reflect signals back onto the **bus**. In order to ensure that the end unit determination circuit and the **bus termination** circuit for each repeater functions even when the repeater is powered off, **termination** power is provided to each repeater in the stack via the stack **bus** connection cable. One of the pins on the stack **bus** connection cable input connector and output connector is dedicated to providing the **termination** voltage and one of the repeaters in the stack is elected to provide power to the **termination** voltage pin.

DEPR:
In one embodiment, termination power is provided by the first unit in the stack
that is powered on. The first unit in the stack that is powered on provides **termination** power to the entire stack **bus and the termination** power is used to provide power to **both the end** unit determination circuit and the **bus termination** circuit in each of the repeaters. In one embodiment, the termination voltage is nominally 5 volts. Because of a switching circuit used to deliver the **termination** voltage to the **bus, in a preferred embodiment, the bus termination** voltage is approximately 4 volts. If the unit providing power

is powered off, then a different unit is elected to provide power to the end unit determination circuits via the stack bus. In general, if any one repeater
unit is turned on, then that repeater unit provides power to the repeater stack
bus so that power may be provided for **bus termination** at the ends of the **bus** regardless of whether or not the repeaters on the ends of the **bus** are powered on.

CCOR:
710/300

CCXR:
326/30

US-CL-CURRENT: 326/30,710/1 ,710/107 ,710/15

US-PAT-NO: 5613074
DOCUMENT-IDENTIFIER: US 5613074 A
TITLE: Automatic disabling of SCSI bus terminators
DATE-ISSUED: March 18, 1997
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Galloway; William C.	Houston	TX	N/A	N/A

US-CL-CURRENT: 710/100,326/30 ,710/1 ,710/107 ,710/15

ABSTRACT:
A system for detecting the presence and size of a SCSI device on a SCSI bus and terminating the SCSI bus accordingly. A SCSI controller is capable of driving two branches of a SCSI bus, each branch having a different data size. When the SCSI controller is at the end of a SCSI chain, termination is enabled,
otherwise termination is disabled. Termination is performed on the portions of
the SCSI data bus requiring termination based on the presence and size of SCSI devices on the branches used.
19 Claims, 7 Drawing figures
Exemplary Claim Number: 6
Number of Drawing Sheets: 7

CLPR:
1. A method for automatically enabling and disabling a SCSI **termination** device
on a SCSI **bus** requiring **termination at both ends** of the SCSI **bus**, the SCSI **bus** having a first and a second data width portion, the SCSI **bus** receiving SCSI devices of first and second data widths, the second data width portion being greater than the first data width portion and including the first data width portion, the method comprising the steps of:

CLPR:
14. An apparatus for automatically **terminating** a SCSI **bus** requiting **termination at both ends** of the SCSI **bus** in a computer system, the SCSI **bus** having a first and a second data width portion, the SCSI **bus** receiving SCSI devices of first and second data widths, the second data width being greater than the first data width and including the first data width, the apparatus comprising:

CLPV:
a SCSI **bus** coupled to said **bus**, said SCSI **bus** requiring **termination at both ends** of the SCSI **bus**, said SCSI **bus** having a first and a second data width portion, said SCSI **bus** for receiving SCSI devices of first and second data widths, the second data width being greater than the first data width and including the first data width;

CCOR:
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CCXR:
326/30

CCXR:

710/1

CCXR:
710/107

CCXR:
710/15

US-CL-CURRENT: **326/30**,**326/86**

US-PAT-NO: 5553250
DOCUMENT-IDENTIFIER: US 5553250 A
TITLE: Bus terminating circuit
DATE-ISSUED: September 3, 1996
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Miyagawa; Takao	Nagaokakyo	N/A	N/A	JPX
Kashio; Akinori	Nagaokakyo	N/A	N/A	JPX
Hashimoto; Ken	Nagaokakyo	N/A	N/A	JPX
Yasuda; Makoto	Nagaokakyo	N/A	N/A	JPX
Sakai; Hidenobu	Nagaokakyo	N/A	N/A	JPX
Kutsche; William C.	Nagaokakyo	N/A	N/A	JPX

US-CL-CURRENT: **710/100**,**326/30** ,**326/86**
ABSTRACT:
A bus terminating circuit is provided on each of a plurality of SCSI devices
connected to each other through an SCSI bus line. A first terminating resistor
is inserted between each of the signal lines and a power source line of the bus
line and a second terminating resistor is inserted between each of the signal lines and ground. A first transistor is connected between the first terminating resistor and the power source line and a second transistor is connected between the second terminating resistor and ground. The first and second transistors are turned-on or off in response to an ON signal or an OFF signal inputted from an external terminal so that the first and second resistors can be connected or disconnected to or from the bus line.
20 Claims, 17 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 15

BSPR:
Next, one example of the SCSI system is shown in FIG. 3. In FIG. 3, reference numerals 2a, 2b, 2c and 2d respectively show the target 2 such as a printer, floppy disk, scanner, hard disk, etc. In a case where a plurality of SCSI devices are connected to each other as shown in FIG. 3, depending on the specification of the SCSI system, the **terminating** resistors of the devices (in the case of FIG. 3, the targets 2a, 2b and 2c) connected between the devices at
both ends (in the case of FIG. 3, the initiator 1 and the target 2d) on the SCSI **bus line** 3 must be disconnected from the **bus line** 3. Conventionally, for connecting/disconnecting the terminating resistors, two methods were known, (i)
a method where mechanical switches such DIP switches are provided at positions shown by the reference symbol A in FIG. 2 and are turned on or off, and (ii) a method where a connector or resistor module which incorporates the terminator 5
(in FIG. 2, the two terminating resistors 5a and 5b between positions denoted by reference symbols B and C) is attached or detached.

BSPR:
In a still further aspect in accordance with the present invention, a **bus terminating** circuit is applied to a **bus line** which includes a power source **line**, ground **line** and first signal **line** and second signal **line** for

transmitting
signals having polarities opposite to each other. In such a case, the **bus terminating** circuit comprises: a regulator having an input terminal connected to the power source **line** and for regulating a voltage inputted to the input end
into a constant voltage to be outputted from an output end thereof; a first **terminating** resistor having one end connected to the output end of the regulator; a second **terminating** resistor having one end connected to the output
end of the regulator; and a third **terminating** resistor having **both ends** connected to another end of the first **terminating** resistor and another end of second **terminating** resistor, respectively.

CCOR:
710/100

CCXR:
326/30

CCXR:
326/86

US-CL-CURRENT: **326/30**,333/17.3 ,333/32 ,**710/2**

US-PAT-NO: 5467455
DOCUMENT-IDENTIFIER: US 5467455 A
TITLE: Data processing system and method for performing dynamic bus termination
DATE-ISSUED: November 14, 1995
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gay; James G.	Pflugerville	TX	N/A	N/A
Ledbetter, Jr.; William B.	Austin	TX	N/A	N/A

US-CL-CURRENT: **710/100**,**326/30** ,333/17.3 ,333/32 ,**710/2**

ABSTRACT:
A data processing system and a method for performing dynamic bus signal termination uses a dynamic bus termination circuitry (14 or 16) with a device (10 or 12). The circuitry is enabled when data is incoming to the device and is disabled when data is outgoing from the device to selectively reduce unwanted signal reflection at the signal end of a bi-directional bus (17). The disabling allows the circuitry to be removed or tristated from any connection with the bus (17) when not needed (i.e., data outgoing) to reduce loading. The disabling of the termination circuitry also aids in reducing the power consumption of the part when either the bus is sitting idle or the part is in a low power mode of operation.
29 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

BSPR:
It is known in the art that devices operating at high speeds, devices operating at high clock frequencies, and/or devices which require extremely long conductive interconnections suffer from a performance-reducing phenomenon referred to as a known and understood signal reflection or transmission line effect problem. If a zero volt signal is changed to a five volt signal, for example, on a conductor or **bus** which is either long in length or operating at a fast edge rate, if the **bus** or conductive **line** is not properly **terminated** via an impedance, the conductive **line or bus** will take time to settle to the 5 volt value from the 0 volt value due to one or more reflections off one or **both ends of the bus**. To reduce signal reflection and thereby improve performance, permanent resistors have been placed at the ends of uni-directional buses to reduce signal reflection. This uni-directional **termination** is easy to do since only one end of the **bus** is ever receiving data (the other end is always sending) and therefore **termination** of the receiving side is all that is required. Unfortunately, if the bus is idle or the part is in a low power mode of operation, the connected permanent resistor usually caused increased power consumption which is disadvantageous.

BSPR:
In a bi-directional **bus, the termination** problem is enhanced because either end
of the **bus** may either be receiving or transmitting at any time. Therefore, in the prior art, permanent resistor **termination** is placed at **both ends of the bus**
and are connected regardless of whether or not they are needed. This results in an increased load to the bus and increased power consumption when the bus is
placed into a low power mode of operation.

DEPR:
The preferred method and apparatus illustrated and taught herein solves the problem of properly **terminating** a bi-directional transmission **line**. Known techniques involved **terminating a bus** at each end of the **bus**, at mid-points on the **bus**, or involve structuring the **bus** in a star-like layout with the **termination** network at the center of the star. There are various known performance disadvantages that occur when using a static **termination on both ends** or mid-point of a **bus**. When allowing a **termination** network to be dynamically switched into or out of a transmission **line** network to place the proper **termination** at the end or final receiver on the **bus** as required, performance is improved.

CCOR:
710/100

CCXR:
326/30

CCXR:
710/2

US-CL-CURRENT: **326/30**,333/17.3 ,333/22R ,333/32 ,**710/2**

US-PAT-NO: 5467453
DOCUMENT-IDENTIFIER: US 5467453 A
TITLE: Circuit for providing automatic SCSI bus termination
DATE-ISSUED: November 14, 1995
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kocis; Thomas	Austin	TX	N/A	N/A

US-CL-CURRENT: **710/300**,**326/30** ,333/17.3 ,333/22R ,333/32 ,**710/2**

ABSTRACT:
Disclosed are a circuit and method for providing automatic termination for a small computer systems interface ("SCSI") bus. The circuit resides within a bus controller comprising (1) a control circuit for controlling transmission of data on a bus and for providing an interface between the bus and a computer system for communication of the data therebetween and (2) a first bus port and a second bus port, each of the first and second bus ports permitting a device to be coupled thereto for communication with the control circuit via the bus, the bus controller being at an end of the bus when a single one of the first and second bus ports is coupled to a device and being in a middle of the bus when both the first and second bus ports are coupled to devices. The circuit of the present invention is coupled to the first and second bus ports and is capable of coupling a terminating circuit to the bus as a function of a presence of devices coupled to the first and second bus ports, the bus requiring coupling of the terminating circuit when the bus controller is at the end of the bus.
36 Claims, 3 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

BSPR:
Some **buses** require **terminating** circuits at each end of the **bus** to provide effective damping. One such bus standard is the small computer systems interface ("SCSI") bus. The SCSI bus is designed to operate in conjunction with microcomputers (also termed personal computers or "PCs") to provide an interface to SCSI standard peripheral devices. SCSI buses require a controller or host card to manage communication of data between the PC and the SCSI devices and between the SCSI devices themselves. In PCs, this controller card is typically placed in a slot within the main chassis of the PC. The controller card contains a control circuit that manages the SCSI bus and at least one SCSI port allowing SCSI devices to couple to the card. SCSI devices are daisy chained together with a common cable. All SCSI devices operate on common signals, and **both ends** of the cable are **terminated** with hardware **terminating** circuits. The **terminating** circuits, that can be connected to either SCSI devices or to the SCSI cable itself are, as stated above, required to make data transfers on the SCSI **bus** reliable.

CCOR:
710/300

CCXR:
326/30

CCXR:
710/2

US-CL-CURRENT: **326/30**,375/257

US-PAT-NO: 5313595
DOCUMENT-IDENTIFIER: US 5313595 A
TITLE: Automatic signal termination system for a computer bus
DATE-ISSUED: May 17, 1994
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lewis; Mark S.	Colorado Springs	CO	N/A	N/A
Ravey; Ronald R.	Colorado Springs	CO	N/A	N/A

US-CL-CURRENT: **710/305**,**326/30** ,375/257

ABSTRACT:
An automatic termination system for an end terminated bus especially useful with the SCSI bus. When utilized with a computer device, for example, a storage subsystem, configuration or reconfiguration of the bus can be automatically effectuated without concerns for inappropriate signal termination of the bus. The invention comprises a circuit which determines if any additional devices have been coupled to the bus and enables an active terminator chip if none is detected. Should another device be coupled onto the bus, the active terminator chip is automatically disabled.
16 Claims, 5 Drawing figures
Exemplary Claim Number: 7
Number of Drawing Sheets: 3

BSPR:
The SCSI **bus** must, however, be **terminated at both ends** (and only at the ends) for proper operation. In fact, the SCSI-2 standard for single ended SCSI recommends active **termination at both ends** of every cable segment. Should the **bus not be terminated** properly, the devices coupled to the **bus** may either cease functioning properly, thereby introducing serious error problems, or cease functioning at all. Conversely, should the SCSI **bus** be "over" **terminated,** i.e. **terminated** at more places than the ends, signal reflections and other signal complications will likewise lead to high failure rates and errors.

CCOR:
710/305

CCXR:
326/30

PGPUB-DOCUMENT-NUMBER: 20010005654
PGPUB-FILING-TYPE: new-utility
DOCUMENT-IDENTIFIER: US 20010005654 A1

TITLE: High speed, high density electrical connector

PUBLICATION-DATE: June 28, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Cohen, Thomas S.	New Boston	NH	US	
Stokoe, Philip T.	Attleboro	MA	US	
McNamara, David M.	Amherst	NH	US	

US-CL-CURRENT: 439/608,439/701

ABSTRACT:

A high speed, high density electrical connector for use with printed circuit boards. The connector is in two pieces with one piece having pins and shield plates and the other having socket type signal contacts and shield plates. The shields have a grounding arrangement which is adapted to control the electromagnetic fields, for various system architectures, simultaneous switching configurations and signal speeds, allowing all of the socket type signal contacts to be used for signal transmission. Additionally, at least one piece of the connector is manufactured from wafers, with each ground plane and signal column injection molded into components which, when combined, form a wafer. This construction allows very close spacing between adjacent columns of signal contacts as well as tightly controlled spacing between the signal contacts and the shields. It also allows for easy and flexible manufacture, such as a connector that has wafers intermixed in a configuration to accommodate single ended, point to point and differential applications.

BSTX:
[0004] Connectors are also used in other configurations for interconnecting printed circuit boards, and even for connecting cables to printed circuit boards. Sometimes, one or more small printed circuit boards are connected to another larger printed circuit board. The larger printed circuit board is called a "mother board" and the printed circuit boards plugged into it are called daughter boards. Also, boards of the same size are sometimes aligned in parallel. **Connectors** used in these applications are sometimes called "stacking **connectors" or "mezzanine connectors."**

US-CL-CURRENT: 439/108

US-PAT-NO: 6293827
DOCUMENT-IDENTIFIER: US 6293827 B1
TITLE: Differential signal electrical connector
DATE-ISSUED: September 25, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stokoe; Philip T.	Attleboro	MA	N/A	N/A

US-CL-CURRENT: 439/608,439/108
ABSTRACT:

A high speed, high density electrical connector. The disclosed embodiments are principally configured for carrying differential signals, though other configurations are discussed. For differential signals, the signal conductors are arranged in pairs and shield strips run parallel to each pair. The connector is manufactured with wafer assemblies. Separate signal and shield wafers are formed. The signal wafers interlock to position signal conductors in pairs and then the shield waters are attached. A cap is placed on the signal wafer assembly to protect contact elements.
20 Claims, 12 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

BSPR:
Connectors are also used in other configurations for interconnecting printed circuit boards, and even for connecting cables to printed circuit boards. Sometimes, one or more small printed circuit boards are connected to another larger printed circuit board. The larger printed circuit board is called a "mother board" and the printed circuit boards plugged into it are called daughter boards. Also, boards of the same size are sometimes aligned in parallel. **Connectors** used in these applications are sometimes called "stacking
connectors" or "mezzanine connectors."

DEPR:
Also, the connector is described in connection with a right angle daughter card
to backplane assembly application. The invention need not be so limited. Similar structures could be used for cable **connectors, mezzanine connectors or connectors** with other shapes.

US-CL-CURRENT: 326/39,340/14.3 ,340/870.18 ,375/341

US-PAT-NO: 6113260
DOCUMENT-IDENTIFIER: US 6113260 A
TITLE: Configurable interface module
DATE-ISSUED: September 5, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Genrich; Thad J.	Aurora	CO	N/A	N/A
Holsteen; David W.	Aurora	CO	N/A	N/A
Martinez; Bruno A.	Westminster	CO	N/A	N/A
Spellman; Daniel L.	Parker	CO	N/A	N/A

US-CL-CURRENT: 714/795,326/39 ,340/14.3 ,340/870.18 ,375/341
ABSTRACT:
A configurable interface module particularly suited for processing of digital and analog information includes at least one field programmable gate array (44, 46, 48) mounted on a mezzanine board (30) to provide functional flexibility and not requiring an additional slot in a computer chassis. In a preferred embodiment, the module is utilized to process weather information and performs the functions of demodulation, bit and frame synchronization, and FIFO buffer control. The gate arrays may be reprogrammed to implement either AM demodulation or BPSK demodulation or adapted to process other types of information, such as telemetry information.
18 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

BSPR:
To further increase flexibility and provide additional processing functions while utilizing a single slot in the chassis, VMEbus carrier boards may include one or more **connectors** to accommodate electronic modules or **mezzanine** boards which may implement a wide variety of control, interface, input/output, analog, and digital functions. One example of such a mezzanine board is the INDUSTRYPACK (IP) manufactured by GreenSpring Computers, Inc. of Menlo Park, Calif.

DEPR:
Referring now to FIG. 1, a typical VMEbus carrier board 10 is illustrated which communicates with a standard backplane (not specifically illustrated) of a chassis (not specifically illustrated) via connector 12. Board 10 may also be connected to various input and output devices via a ribbon cable 14 or the like. Board 10 includes at least one mechanical **connector, such as connectors** 16 and 18 which are adapted to receive corresponding **connectors** 19 on single **mezzanine** boards 20 and 22. Fasteners 24 may be used to secure mezzanine boards 20 and 22 to carrier board 10. The particular carrier board illustrated is referred to as a 3U or single VMEbus carrier board. In a preferred embodiment, a 6U or double VMEbus carrier board which accommodates two (2) double mezzanine boards (or four (4) single mezzanine boards).

CLPV:

a **mezzanine** board having at least one **connector** to mechanically and electrically link the **mezzanine** board to the carrier board; and

CLPV:
a **mezzanine** board having at least one **connector** to mechanically and electrically link the **mezzanine** board to the carrier board; and

L Number	Hits	Search Text	DB	Time stamp
1	739	326/30.ccls.	USPAT; US-PGPUB	2001/11/28 10:51
4	698	710/100.ccls.	USPAT; US-PGPUB	2001/11/28 10:52
7	16	326/30.ccls. and 710/100.ccls.	USPAT; US-PGPUB	2001/11/28 11:00
10	213545	resistor$1	USPAT; US-PGPUB	2001/11/28 11:44
13	26251	25$ with 65$	USPAT; US-PGPUB	2001/11/28 11:14
14	0	("25" adj ohms) near5 ("65" adj ohms)	USPAT; US-PGPUB	2001/11/28 11:15
17	2	("25" adj2 ohms) near5 ("65" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:20
20	0	("25" adj2 ohms) near5 ("65" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:20
25	0	("25" adj3 ohms) near10 ("65" adj3 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:20
30	6	("25" adj3 ohms) near10 ("65" adj3 ohms)	USPAT; US-PGPUB	2001/11/28 11:22
33	365	resistor$1 same (25$ with 65$)	USPAT; US-PGPUB	2001/11/28 11:22
36	0	(326/30.ccls. and 710/100.ccls.) and (resistor$1 same (25$ with 65$))	USPAT; US-PGPUB	2001/11/28 11:23
39	16	(326/30.ccls. and 710/100.ccls.) and 326/30.ccls.	USPAT; US-PGPUB	2001/11/28 11:23
42	1	(resistor$1 same (25$ with 65$)) and 326/30.ccls.	USPAT; US-PGPUB	2001/11/28 11:24
45	1	(resistor$1 same (25$ with 65$)) and "2"	USPAT; US-PGPUB	2001/11/28 11:24
48	0	(resistor$1 same (25$ with 65$)) and 710/100.ccls.	USPAT; US-PGPUB	2001/11/28 11:24
51	50119	terminat$ with (line$1 or bus or buses or busses)	USPAT; US-PGPUB	2001/11/28 11:44
54	16	(326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))	USPAT; US-PGPUB	2001/11/28 11:30
57	16	((326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))) and resistor$1	USPAT; US-PGPUB	2001/11/28 11:33
60	763	"about" near5 ("50" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:45
63	0	(((326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))) and resistor$1) and ("about" near5 ("50" adj2 ohms))	USPAT; US-PGPUB	2001/11/28 11:37
66	26	(terminat$ with (line$1 or bus or buses or busses)) same ("about" near5 ("50" adj2 ohms))	USPAT; US-PGPUB	2001/11/28 11:37
69	9	resistor$1 same ((terminat$ with (line$1 or bus or buses or busses)) same ("about" near5 ("50" adj2 ohms)))	USPAT; US-PGPUB	2001/11/28 11:37
72	14069	terminat$ with (line$1 or bus or buses or busses)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
77	246378	resistor$1	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
82	21	"about" near5 ("50" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
87	0	(terminat$ with (line$1 or bus or buses or busses)) same resistor$1 same ("about" near5 ("50" adj2 ohms))	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:46
92	1246	(terminat$ with (line$1 or bus or buses or busses)) same resistor$1	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:46

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97	11	(terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:58
102	283	(terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:59
105	570	"7" adj3 "12" adj3 (percent or "%")	USPAT; US-PGPUB	2001/11/28 12:01
108	0	((terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)) same ("7" adj3 "12" adj3 (percent or "%"))	USPAT; US-PGPUB	2001/11/28 12:01
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120	0	6067594.ref.	USPAT; US-PGPUB	2001/11/28 13:28
123	1	6067594.pn.	USPAT; US-PGPUB	2001/11/28 13:46
126	1		USPAT	2001/11/28 13:29
127	1		USPAT	2001/11/28 13:29
128	1		USPAT	2001/11/28 13:30
129	1		USPAT	2001/11/28 13:30
130	1		USPAT	2001/11/28 13:30
131	1		USPAT	2001/11/28 13:31
132	1		USPAT	2001/11/28 13:31
133	1		USPAT	2001/11/28 13:31
134	1		USPAT	2001/11/28 13:32
135	1		USPAT	2001/11/28 13:32
136	1		USPAT	2001/11/28 13:33
137	1		USPAT	2001/11/28 13:33
138	1		USPAT	2001/11/28 13:33
139	1		USPAT	2001/11/28 13:33
140	1		USPAT	2001/11/28 13:34
141	1		USPAT	2001/11/28 13:34
142	1		USPAT	2001/11/28 13:34
143	1		USPAT	2001/11/28 13:42
144	1		USPAT	2001/11/28 13:42
145	1		USPAT	2001/11/28 13:43
146	139	rambus.asn.	USPAT; US-PGPUB	2001/11/28 13:47
149	58	(terminat$ with (line$1 or bus or buses or busses)) and rambus.asn.	USPAT; US-PGPUB	2001/11/28 13:48

L Number	Hits	Search Text	DB	Time stamp
1	739	326/30.ccls.	USPAT; US-PGPUB	2001/11/28 10:51
4	698	710/100.ccls.	USPAT; US-PGPUB	2001/11/28 10:52
7	16	326/30.ccls. and 710/100.ccls.	USPAT; US-PGPUB	2001/11/28 11:00
10	213545	resistor$1	USPAT; US-PGPUB	2001/11/28 11:44
13	26251	25$ with 65$	USPAT; US-PGPUB	2001/11/28 11:14
14	0	("25" adj ohms) near5 ("65" adj ohms)	USPAT; US-PGPUB	2001/11/28 11:15
17	2	("25" adj2 ohms) near5 ("65" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:20
20	0	("25" adj2 ohms) near5 ("65" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:20
25	0	("25" adj3 ohms) near10 ("65" adj3 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:20
30	6	("25" adj3 ohms) near10 ("65" adj3 ohms)	USPAT; US-PGPUB	2001/11/28 11:22
33	365	resistor$1 same (25$ with 65$)	USPAT; US-PGPUB	2001/11/28 11:22
36	0	(326/30.ccls. and 710/100.ccls.) and (resistor$1 same (25$ with 65$))	USPAT; US-PGPUB	2001/11/28 11:23
39	16	(326/30.ccls. and 710/100.ccls.) and 326/30.ccls.	USPAT; US-PGPUB	2001/11/28 11:23
42	1	(resistor$1 same (25$ with 65$)) and 326/30.ccls.	USPAT; US-PGPUB	2001/11/28 11:24
45	1	(resistor$1 same (25$ with 65$)) and "2"	USPAT; US-PGPUB	2001/11/28 11:24
48	0	(resistor$1 same (25$ with 65$)) and 710/100.ccls.	USPAT; US-PGPUB	2001/11/28 11:24
51	50119	terminat$ with (line$1 or bus or buses or busses)	USPAT; US-PGPUB	2001/11/28 11:44
54	16	(326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))	USPAT; US-PGPUB	2001/11/28 11:30
57	16	((326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))) and resistor$1	USPAT; US-PGPUB	2001/11/28 11:33
60	763	"about" near5 ("50" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:45
63	0	(((326/30.ccls. and 710/100.ccls.) and (terminat$ with (line$1 or bus or buses or busses))) and resistor$1) and ("about" near5 ("50" adj2 ohms))	USPAT; US-PGPUB	2001/11/28 11:37
66	26	(terminat$ with (line$1 or bus or buses or busses)) same ("about" near5 ("50" adj2 ohms))	USPAT; US-PGPUB	2001/11/28 11:37
69	9	resistor$1 same ((terminat$ with (line$1 or bus or buses or busses)) same ("about" near5 ("50" adj2 ohms)))	USPAT; US-PGPUB	2001/11/28 11:37
72	14069	terminat$ with (line$1 or bus or buses or busses)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
77	246378	resistor$1	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
82	21	"about" near5 ("50" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:45
87	0	(terminat$ with (line$1 or bus or buses or busses)) same resistor$1 same ("about" near5 ("50" adj2 ohms))	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:46
92	1246	(terminat$ with (line$1 or bus or buses or busses)) same resistor$1	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:46

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97	11	(terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:58
102	283	(terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:59
105	570	"7" adj3 "12" adj3 (percent or "%")	USPAT; US-PGPUB	2001/11/28 12:01
108	0	((terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)) same ("7" adj3 "12" adj3 (percent or "%"))	USPAT; US-PGPUB	2001/11/28 12:01
111	0	((terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms)) and ("7" adj3 "12" adj3 (percent or "%"))	USPAT; US-PGPUB	2001/11/28 12:02
114	2	percent$ same ((terminat$ with (line$1 or bus or buses or busses)) same impedance same ("50" adj2 ohms))	USPAT; US-PGPUB	2001/11/28 12:46

	Document ID	Issue Date	Title
1	US 6308232 B1	20011023	Electronically moveable terminator and method for using same in a memory system
2	US 6272577 B1	20010807	Data processing system with master and slave devices and asymmetric signal swing bus
3	US 6122695 A	20000919	Device for terminating a processor bus
4	US 6078978 A	20000620	Bus interface circuit in a semiconductor memory device
5	US 6067596 A	20000523	Flexible placement of GTL end points using double termination points
6	US 6029216 A	20000222	Auto-termination method and apparatus for use with either active high or active low terminators
7	US 6026456 A	20000215	System utilizing distributed on-chip termination
8	US 5919252 A	19990706	Process and apparatus for adaptive bus termination
9	US 5903736 A	19990511	Method and apparatus for smooth inductive compensation of transmission bus capacitive parasitics
10	US 5864715 A	19990126	System for automatically terminating a daisy-chain peripheral bus with either single-ended or differential termination network depending on peripheral bus signals and peripheral device interfaces
11	US 5634014 A	19970527	Semiconductor process, power supply voltage and temperature compensated integrated system bus termination
12	US 5613074 A	19970318	Automatic disabling of SCSI bus terminators
13	US 5596757 A	19970121	System and method for selectively providing termination power to a SCSI bus terminator from a host device

	Current OR	Current XRef
1	710/100	326/30
2	710/110	326/121 ; 326/21 ; 326/30 ; 326/80 ; 326/81 ; 326/83 ; 326/86 ; 327/309 ; 710/100 ; 710/107
3	710/100	326/30 ; 710/301 ; 712/1
4	710/305	326/30 ; 710/100
5	710/306	326/30 ; 370/402 ; 710/100
6	710/100	326/30
7	710/100	326/30 ; 326/86
8	710/100	326/30
9	710/100	326/30
10	710/63	326/30 ; 710/100 ; 710/62
11	710/100	326/30
12	710/100	326/30 ; 710/1 ; 710/107 ; 710/15
13	713/324	326/30 ; 333/32 ; 710/100 ; 710/2

	Document ID	Issue Date	Title
14	US 5553250 A	19960903	Bus terminating circuit
15	US 5495584 A	19960227	SCSI bus concatenator/splitter
16	US 5467455 A	19951114	Data processing system and method for performing dynamic bus termination

	Current OR	Current XRef
14	710/100	326/30 ; 326/86
15	710/316	326/30 ; 370/254 ; 710/100
16	710/100	326/30 ; 333/17.3 ; 333/32 ; 710/2

US006308232B1

(12) **United States Patent**
Gasbarro

(10) **Patent No.: US 6,308,232 B1**
(45) **Date of Patent: Oct. 23, 2001**

(54) **ELECTRONICALLY MOVEABLE TERMINATOR AND METHOD FOR USING SAME IN A MEMORY SYSTEM**

(75) Inventor: **James Anthony Gasbarro**, Mountain View, CA (US)

(73) Assignee: **Rambus Inc.**, Los Altos, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/387,842**

(22) Filed: **Sep. 1, 1999**

(51) **Int. Cl.**[7] **G06F 13/00**

(52) **U.S. Cl.** **710/100**; 326/30

(58) **Field of Search** 710/100, 101, 710/102, 103, 104; 326/30; 711/100, 170

(56) **References Cited**

U.S. PATENT DOCUMENTS

Re. 36,789	*	7/2000	Mandel et al.	326/30
5,313,595	*	5/1994	Lewis et al.	710/126
5,382,841	*	1/1995	Feldbaumer	326/30
5,635,852	*	6/1997	Wallace	326/30
6,029,216	*	2/2000	Hoglund et al.	710/101
6,100,713	*	8/2000	Kalb et al.	326/30

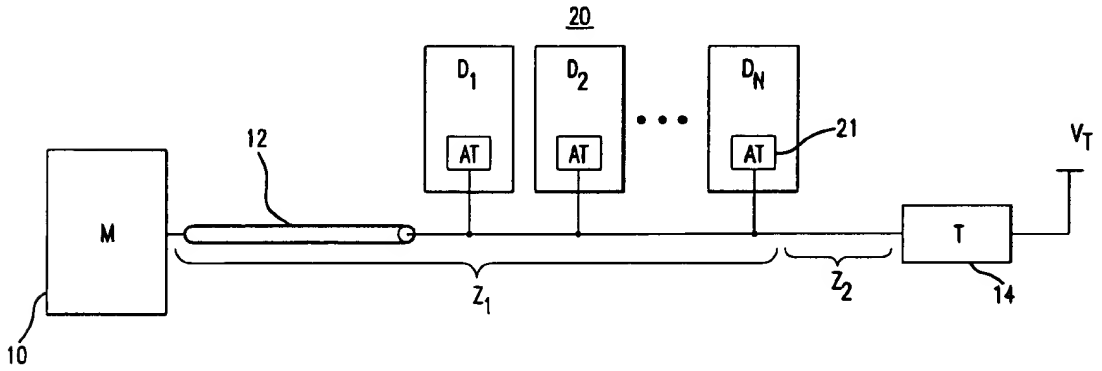
* cited by examiner

Primary Examiner—Glenn A. Auve

(57) **ABSTRACT**

An expandable memory system having a plurality of memory devices, each with an electronically activated terminator is disclosed. Also a method for detecting the last memory device arranged along a data bus connecting a memory controller with the memory devices, and activating its active terminator is disclosed.

17 Claims, 7 Drawing Sheets



US006272577B1

(12) **United States Patent**
Leung et al.

(10) **Patent No.: US 6,272,577 B1**
(45) **Date of Patent: Aug. 7, 2001**

(54) **DATA PROCESSING SYSTEM WITH MASTER AND SLAVE DEVICES AND ASYMMETRIC SIGNAL SWING BUS**

(75) Inventors: **Wingyu Leung**, Cupertino; **Winston Lee**, South San Francisco; **Fu-Chieh Hsu**, Saratoga, all of CA (US)

(73) Assignee: **Monolithic System Technology, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/960,951**

(22) Filed: **Oct. 30, 1997**

Related U.S. Application Data

(62) Division of application No. 08/549,610, filed on Oct. 27, 1995, now Pat. No. 5,729,152, which is a division of application No. 08/270,856, filed on Jul. 5, 1994, now Pat. No. 5,655,113.

(51) **Int. Cl.**[7] **G06F 13/00**

(52) **U.S. Cl.** **710/110**; 710/100; 710/107; 710/128; 326/21; 326/30; 326/80; 326/81; 326/83; 326/86; 326/121; 327/309

(58) **Field of Search** 710/100, 107, 710/110, 128; 326/80, 81, 83, 86, 121, 21, 30; 327/309

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,585,378	6/1971	Bouricius et al.	371/51.1
3,651,473	3/1972	Faber	395/281
3,761,879	9/1973	Brandsma et al.	395/292

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

0 178 949	4/1986	(EP) .
0 389 203	9/1990	(EP) .
59-212962	12/1984	(JP) .

(List continued on next page.)

OTHER PUBLICATIONS

Peter van Zant, *Microchip, A Practical Guide to Semiconductor Processing*, 1st Ed., Semiconductor Services, San Jose, CA 1986, p. 8.

MacDonald et al., "Dynamic RAMs 200mb Wafer Memory," IEEE *ISSCC*, Feb. 17, 1989, pp. 240–241 and 350.

Cavil et al., "Wafer–Scale Integratrion," *Micro–electronics Manufacturing Technology*, May, 1991, pp. 55–59.

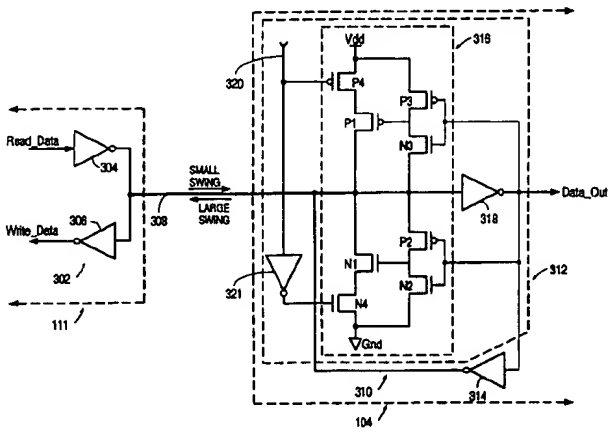
(List continued on next page.)

Primary Examiner—Ayaz Sheikh
Assistant Examiner—Frantz B. Jean
(74) *Attorney, Agent, or Firm*—Skjerven Morrill MacPherson LLP; Norman R. Klivans; Signe M. Holmbeck

(57) **ABSTRACT**

A memory device which utilizes a plurality of memory modules coupled in parallel to a master I/O module through a single directional asymmetrical signal swing (DASS) bus. This structure provides an I/O scheme having symmetrical swing around half the supply voltage, high through-put, high data bandwidth, short access time, low latency and high noise immunity. The device utilizes improved column access circuitry including an improved address sequencing circuit and a data amplifier within each memory module. A resynchronization circuit allows the device to operate either synchronously and asynchronously using the same pins. Each memory module has independent address and command decoders to enable independent operation so that each memory module is activated by commands on the DASS bus only when a memory access operation is performed within the particular memory module. Redundant memory modules are included to replace defective memory modules, and replacement can be carried out through commands on the DASS bus. The memory device can be configured to simultaneously write a single input data stream to multiple memory modules or to perform high-speed interleaved read and write operations. In one embodiment, multiple memory devices are coupled to a common, high-speed I/O bus without requiring large bus drivers and complex bus receivers in the memory modules.

49 Claims, 24 Drawing Sheets



US006122695A

United States Patent [19]

Cronin

[11] Patent Number: 6,122,695

[45] Date of Patent: *Sep. 19, 2000

[54] **DEVICE FOR TERMINATING A PROCESSOR BUS**

[75] Inventor: **Jeffrey J. Cronin**, Blaine, Minn.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: This patent is subject to a terminal disclaimer.

[21] Appl. No.: **09/025,722**

[22] Filed: **Feb. 18, 1998**

[51] **Int. Cl.**[7] **G06F 13/38**; G06F 13/40

[52] **U.S. Cl.** **710/126**; 710/128; 710/129; 710/101; 712/1; 326/30; 375/36

[58] **Field of Search** 710/126, 129, 710/101, 128; 712/1; 326/30; 375/36

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,660,141	4/1987	Ceccon et al.	364/200
5,096,090	3/1992	Schwartz	221/125
5,239,559	8/1993	Brach et al.	375/36
5,367,697	11/1994	Barlow et al.	712/1
5,467,455	11/1995	Gay et al.	710/101
5,473,264	12/1995	Mader et al.	326/30
5,495,584	2/1996	Holman, Jr. et al.	710/128
5,585,741	12/1996	Jordan	326/30
5,629,831	5/1997	Eggert et al.	361/624
5,706,447	1/1998	Vivio	710/129
5,748,910	5/1998	Herrera	710/101

OTHER PUBLICATIONS

"FIC PA–2007 Motherboard," *Computer Source Magazine*, pp. 54–55, Oct. 1997 (best copy).

Metz, Cade, "Pentium PART II," *PC Magazine*, pp. 100–104, Jun. 1997.

Metz, Cade, "Pentium Part II", *PC Magazine*, Jun. 10, 1997, pp. 100–104.

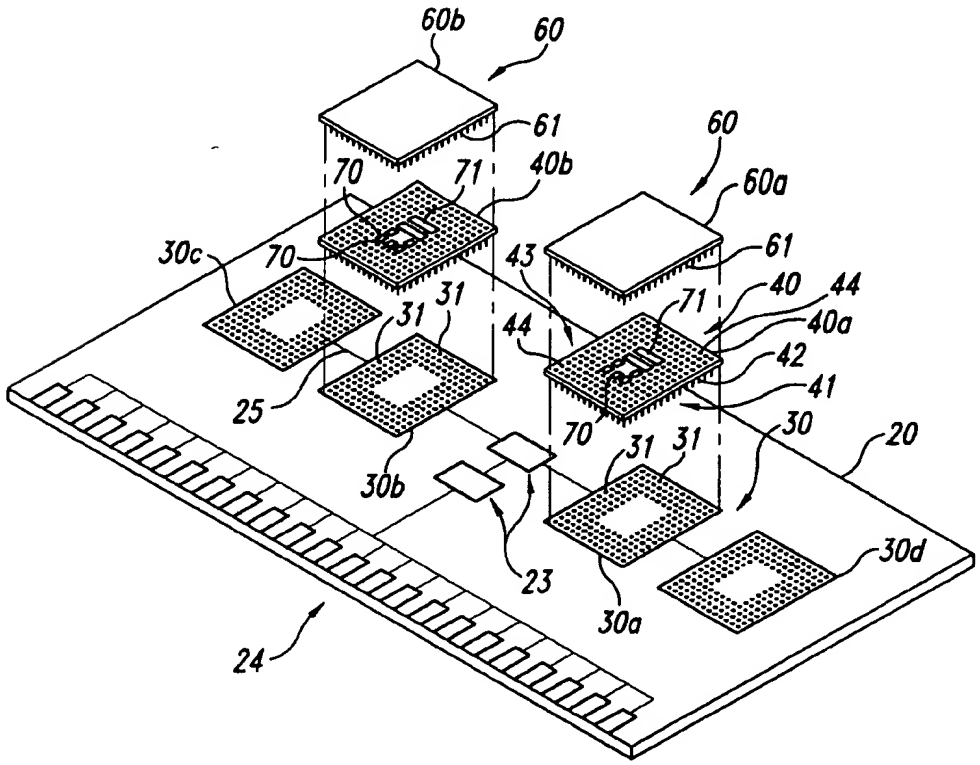
"Hot New Product—FIC PA–207 Motherboard—First International Computer is one of the first to manufacture a motherboard with 1 MB of Cache," *Computer Source Magazine*, Oct. 1997, pp. 54–55.

Primary Examiner—Ayaz R. Sheikh
Assistant Examiner—Frantz Blanchard Jean
Attorney, Agent, or Firm—Perkins Coie LLP

[57] **ABSTRACT**

A device for terminating a bus configured to have one or more processors coupled thereto. The device comprises a support member having a termination circuit which is coupled to a conductor of the bus when the support member is coupled to the bus. In one embodiment, the support member is coupled between the bus and the processor. In another embodiment, the support member is connected to the bus separately from the processor. The support member may include an auxiliary circuit in addition to the termination circuit which may be used to correct, supply, or update signals transmitted on the bus.

56 Claims, 6 Drawing Sheets



US006078978A

United States Patent [19]

Suh

[11] Patent Number: 6,078,978

[45] Date of Patent: Jun. 20, 2000

[54] **BUS INTERFACE CIRCUIT IN A SEMICONDUCTOR MEMORY DEVICE**

[75] Inventor: **Jung Won Suh**, Kyungki-do, Rep. of Korea

[73] Assignee: **Hyundai Electronics Industries Co., Ltd.**, Kyoungki-do, Rep. of Korea

[21] Appl. No.: **09/098,729**

[22] Filed: **Jun. 18, 1998**

[30] **Foreign Application Priority Data**

Jun. 20, 1997 [KR] Rep. of Korea 97-26186

[51] **Int. Cl.**[7] **G06F 13/00**

[52] **U.S. Cl.** **710/129**; 710/126; 710/128; 710/100; 326/30

[58] **Field of Search** 710/128, 126, 710/129, 100; 326/30

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,634,014 5/1997 Gist et al. 395/280

5,687,330 11/1997 Gist et al. 710/129

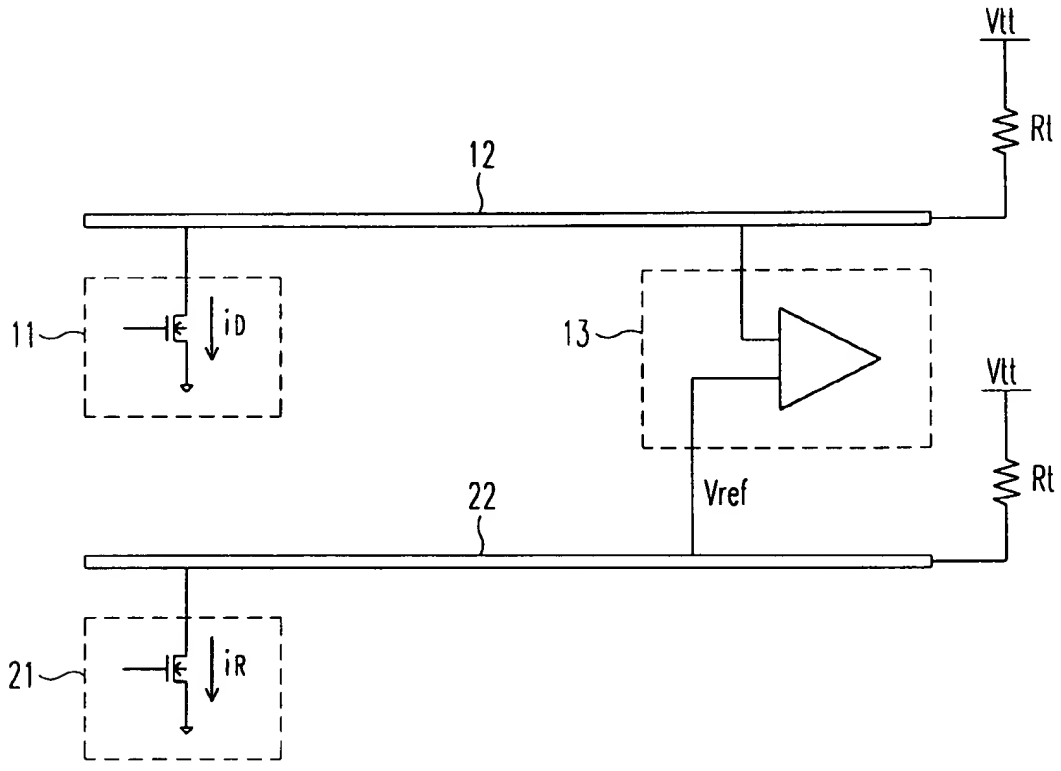
Primary Examiner—Ario Etienne

Attorney, Agent, or Firm—Nath & Associates; Gary M. Nath; Harold L. Novick

[57] **ABSTRACT**

This invention relates to a bus interface circuit in a semiconductor memory device. This invention comprises a data driver to transmit a data signal through a first transmission line of which one end is terminated; a reference voltage driver to transmit a reference voltage signal through a second transmission line of which one end is terminated; and a receiver to determine a logic state by comparing the data signal transmitted by the first transmission line with the reference voltage signal transmitted by the second transmission line. Accordingly, a high-speed bus interface circuit of the present invention can decrease a common mode noise, influence of ground bounce, an output voltage swing and a power consumption by simultaneously driving a data driver and a reference voltage driver in a memory interface using a transmission line being either single or parallel terminated to transmit to a receiver.

5 Claims, 6 Drawing Sheets



US006078978A

United States Patent [19]

Suh

[11] Patent Number: 6,078,978

[45] Date of Patent: Jun. 20, 2000

[54] **BUS INTERFACE CIRCUIT IN A SEMICONDUCTOR MEMORY DEVICE**

[75] Inventor: **Jung Won Suh**, Kyungki-do, Rep. of Korea

[73] Assignee: **Hyundai Electronics Industries Co., Ltd.**, Kyoungki-do, Rep. of Korea

[21] Appl. No.: **09/098,729**

[22] Filed: **Jun. 18, 1998**

[30] **Foreign Application Priority Data**

Jun. 20, 1997 [KR] Rep. of Korea 97-26186

[51] **Int. Cl.**[7] **G06F 13/00**

[52] **U.S. Cl.** **710/129**; 710/126; 710/128; 710/100; 326/30

[58] **Field of Search** 710/128, 126, 710/129, 100; 326/30

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,634,014 5/1997 Gist et al. 395/280

5,687,330 11/1997 Gist et al. 710/129

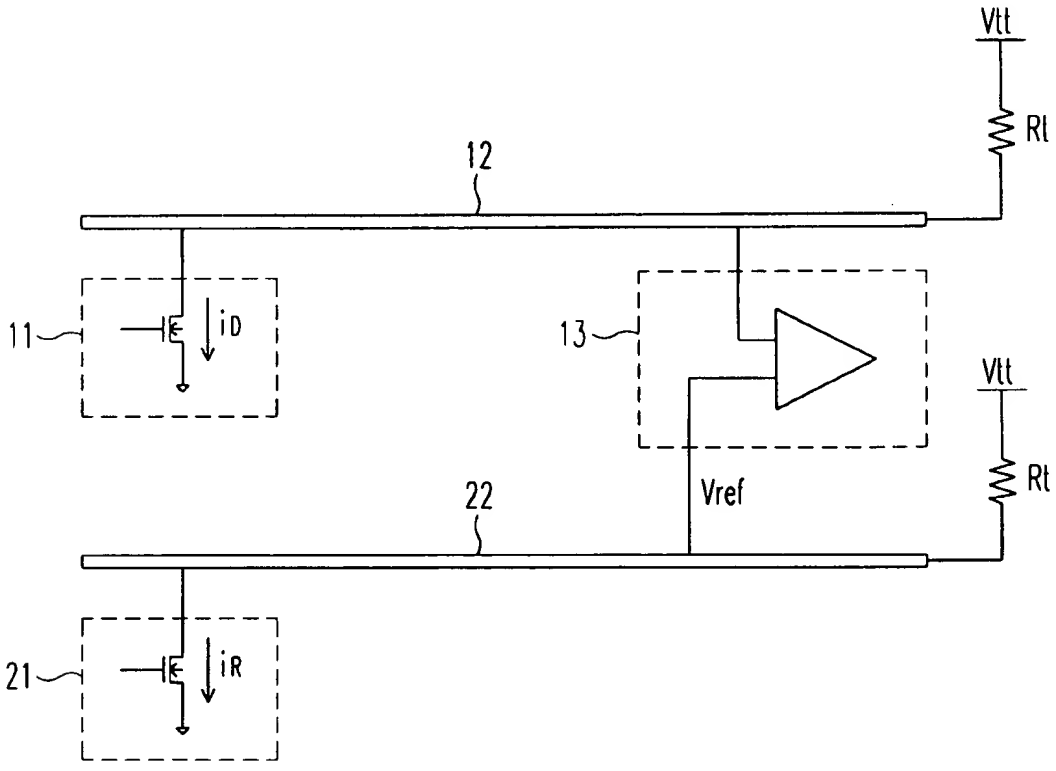
Primary Examiner—Ario Etienne

Attorney, Agent, or Firm—Nath & Associates; Gary M. Nath; Harold L. Novick

[57] **ABSTRACT**

This invention relates to a bus interface circuit in a semiconductor memory device. This invention comprises a data driver to transmit a data signal through a first transmission line of which one end is terminated; a reference voltage driver to transmit a reference voltage signal through a second transmission line of which one end is terminated; and a receiver to determine a logic state by comparing the data signal transmitted by the first transmission line with the reference voltage signal transmitted by the second transmission line. Accordingly, a high-speed bus interface circuit of the present invention can decrease a common mode noise, influence of ground bounce, an output voltage swing and a power consumption by simultaneously driving a data driver and a reference voltage driver in a memory interface using a transmission line being either single or parallel terminated to transmit to a receiver.

5 Claims, 6 Drawing Sheets



US006067596A

United States Patent [19]

Nguyen et al.

[11] Patent Number: 6,067,596

[45] Date of Patent: May 23, 2000

[54] **FLEXIBLE PLACEMENT OF GTL END POINTS USING DOUBLE TERMINATION POINTS**

[75] Inventors: **Thu Q. Nguyen**, Tomball; **Hung Q. Phu**, Friendswood, both of Tex.

[73] Assignee: **Compaq Computer Corporation**, Houston, Tex.

[21] Appl. No.: **09/153,821**

[22] Filed: **Sep. 15, 1998**

[51] **Int. Cl.**[7] **G06F 13/00**

[52] **U.S. Cl.** **710/129**; 710/100; 326/30; 370/402

[58] **Field of Search** 710/129, 131, 710/100, 2, 126; 326/30; 709/300, 400; 712/10; 711/105, 148; 370/285, 402, 911; 713/400; 714/1

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,715,921	12/1987	Maher et al. .	
4,910,593	3/1990	Well .	
5,013,385	5/1991	Maher et al. .	
5,029,284	7/1991	Feldbaumer et al.	307/443
5,596,757	1/1997	Smith	395/750
5,701,422	12/1997	Kirkland, Jr. et al. .	
5,706,447	1/1998	Vivio	395/309
5,729,154	3/1998	Taguchi et al.	326/30

OTHER PUBLICATIONS

100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel 440BX AGPset, AP–827 Application Note, Copyright © Intel Corporation 1997, Order No. 243735–001, pp. 1–34.

Pentium® II Xeon™ Processor AT 400 MHz, Copyright © Intel Corporation, Jun. 1998, Order No. 243770–001, pp. 1–96.

Pentium® Xeon™ Processor/Intel ® 450NX PCIset AGTL+ Layout Guidelines, AP–830 Application Note, Copyright © Intel Corporation, Jun. 1998, Order No. 243790–001, pp. 1–29.

100 MHz 2–Way SMP Pentium® II Xeon™ Processor/ Intel® 440GX AGPset AGTL+ Layout Guidelines, AP–829 Application Note, Copyright© Intel Corporation, Jun. 1998, ORder No. 243775–001, pp. 1–29.

Intel® Pentium® II Xeon™ Processor Bus Terminator Design Guidelines, Copyright © Intel Corporation, Jul. 1998, Order No. 243774–001, pp. 1–11.

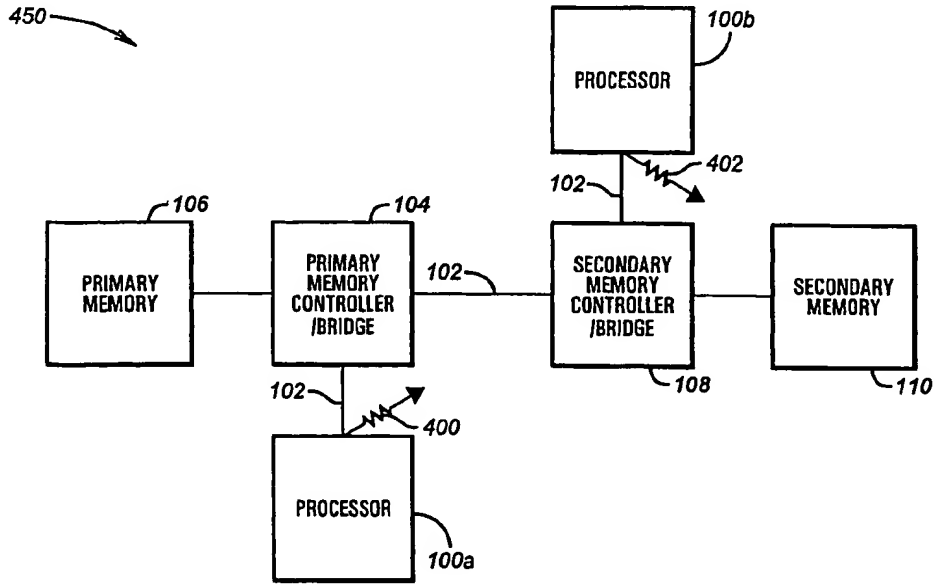
Primary Examiner—Gopal C. Ray

Attorney, Agent, or Firm—Akin, Gump, Strauss, Hauer & Feld, LLP

[57] **ABSTRACT**

A highly parallel computer system including dual processors and dual memory controllers are coupled to an Assisted Gunning Transceiver Logic Plus (AGTL+) high speed system bus. The microprocessors are designed for a quad processor architecture requiring four processors and four connectors for the processors. To maintain signal timing and integrity in a dual processor/dual memory controller architecture, additional terminations are inserted. Printed circuit board space is conserved with a dual processor architecture. The additional connectors and traces to the additional connectors for the processors are no longer needed. Furthermore, with the dual processor design, there is no need for two additional termination cards.

20 Claims, 4 Drawing Sheets



US006029216A

United States Patent [19]

Hoglund et al.

[11] Patent Number: 6,029,216

[45] Date of Patent: Feb. 22, 2000

[54] **AUTO-TERMINATION METHOD AND APPARATUS FOR USE WITH EITHER ACTIVE HIGH OR ACTIVE LOW TERMINATORS**

[75] Inventors: **Timothy E. Hoglund**, Colorado Springs, Colo.; **Erich S. Otto**, Neuried, Germany

[73] Assignee: **LSI Logic Corporation**, Milpitas, Calif.

[21] Appl. No.: **08/884,233**

[22] Filed: **Jun. 27, 1997**

[51] **Int. Cl.**[7] **G06F 13/00**

[52] **U.S. Cl.** **710/101**; 326/30

[58] **Field of Search** 395/281, 306; 326/30

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,220,876	9/1980	Ray	307/296
4,367,525	1/1983	Brown	364/200
4,748,426	5/1988	Stewart	333/22
4,831,283	5/1989	Newton	307/443
4,920,339	4/1990	Friend et al.	340/825.52
4,965,723	10/1990	Kirk et al.	364/200
5,029,284	7/1991	Feldbaumer et al.	307/443
5,099,137	3/1992	Lattin, Jr.	307/147
5,101,481	3/1992	Anger et al.	395/325
5,120,909	6/1992	Kutz et al.	178/63 R
5,157,771	10/1992	Losi et al.	395/325
5,191,581	3/1993	Woodbury et al.	370/85.9
5,204,669	4/1993	Dorfe et al.	340/825.52
5,239,559	8/1993	Brach et al.	375/36
5,239,658	8/1993	Yamamuro et al.	395/800
5,265,038	11/1993	Kowk	364/572
5,313,105	5/1994	Samela et al.	307/99
5,313,595	5/1994	Lewis et al.	395/325
5,327,114	7/1994	Straate et al.	340/286.06
5,338,979	8/1994	Mammano et al.	307/443
5,367,647	11/1994	Coulson et al.	395/325
5,382,841	1/1995	Feldbaumer	326/30
5,410,141	4/1995	Koenck et al.	235/472
5,422,580	6/1995	Mandel et al.	326/30
5,434,516	7/1995	Kosco	326/30

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

0531630	3/1993	European Pat. Off.	G06F 13/40
0076921	4/1993	European Pat. Off.	G06F 11/34
0645716	3/1995	European Pat. Off.	G06F 13/40
0671691	9/1995	European Pat. Off.	G06F 13/12
0742612	11/1996	European Pat. Off.	H01R 43/26
1014624	of 0000	Japan .	
1259442	of 0000	Japan .	
5224792	of 0000	Japan .	
9408035	4/1994	WIPO	G06F 13/40

OTHER PUBLICATIONS

VLSI and Computer Peripherals, Hamburg; May 8–12, 1989; W. Proebster et al.; VLSI Based Tools for Monitoring Bus Communication Channels; pp. 4–81–84.

"Automatic Small Computer–System Interface Termination Circuit for Narrow/Wide Devices on Wide Bus" IBM Technical Disclosure Bulletin. vol. 40, No. 4, Apr. 1997, New York, US, pp. 79–82, XP000728275.

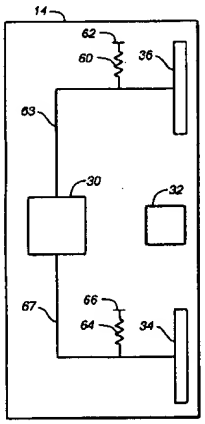
Primary Examiner—Ayaz R. Sheikh

Assistant Examiner—David A. Wiley

[57] **ABSTRACT**

An auto-termination method and apparatus for use with either active high or active low terminators are disclosed. The method includes the steps of (a) forcing a terminator to a first state by impressing a first voltage upon an input of the terminator; (b) determining, from the first voltage, a second voltage that when applied to the input of the terminator places the terminator in a second state; and (c) selectively forcing the terminator to the second state by impressing the second voltage upon the input of the terminator. The apparatus includes a terminator and a controller. The terminator is coupled to the bus and includes an input that is coupled to a first voltage that forces the terminator to a first state. The controller is coupled to the input of the terminator and is configured to determine the voltage of the first voltage coupled to the input of the terminator and to selectively force the terminator to a second state by impressing a second voltage upon the input of the terminator that is different than the first voltage.

18 Claims, 2 Drawing Sheets



US006026456A

United States Patent [19]

Ilkbahar

[11] Patent Number: 6,026,456

[45] Date of Patent: *Feb. 15, 2000

[54] SYSTEM UTILIZING DISTRIBUTED ON-CHIP TERMINATION

[75] Inventor: Alper Ilkbahar, Santa Cruz, Calif.

[73] Assignee: Intel Corporation, Santa Clara, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: 08/573,568

[22] Filed: Dec. 15, 1995

[51] Int. Cl.[7] H03K 17/16; H03K 19/094; G06F 13/00

[52] U.S. Cl. 710/101; 326/30; 326/86

[58] Field of Search 326/30, 86; 395/281; 333/22

[56] References Cited

U.S. PATENT DOCUMENTS

4,120,029	10/1978	Steiner	395/182.13
4,942,398	7/1990	Peterson	326/30
5,023,488	6/1991	Gunning	307/475
5,134,311	7/1992	Biber et al.	326/30
5,214,320	5/1993	Truong	326/30
5,298,800	3/1994	Dunlop et al.	307/270
5,347,177	9/1994	Lipp	307/443
5,497,113	3/1996	Uber	326/27
5,498,990	3/1996	Leung et al.	326/30
5,546,016	8/1996	Allen	326/30
5,568,046	10/1996	Samela et al.	326/30
5,596,757	1/1997	Smith	326/30
5,635,852	6/1997	Wallace	326/30
5,687,330	11/1997	Gist et al.	326/30
5,689,655	11/1997	Tanaka et al.	326/30
5,767,695	6/1998	Takekurka et al.	326/30

OTHER PUBLICATIONS

"GTL:A Low Voltage Swing Transmission Line Tranceiver"pp. 1–6 (Mar. 1991).

T. Knight, Jr. et al. "A Self-Terminating Low-Voltage Swing CMOS Output Driver", *IEEE Journal of Solid-State Circuits*, vol. 23, No. 2, pp. 457–464 (Apr. 1988).

T. Kawahara et al. "Complementary Selective Writing by Direct-Write E-Beam/Optical Lithography Using Mixed Positive and Negative Resist", Symposium on VLSI Circuits Digest of Technical Papers, 4.6, pp. 45–46 (1994).

T. Saton, *Fujitsu Terminated LVTTL (CTT) Presentation*, (May 1993).

D. Fenwick, et al., "The AlphaServer 8000 Series: High-end Server Platform Development ", Copyright 1995 Digital Equipment Corporation.

M. Dolle, "A Dynamic Line-Termination Circuit for Multireceiver Nets", *IEEE Journal on Solid-State Circuits*, vol. 28., No.12, pp. 1370–1373 (Dec. 1993).

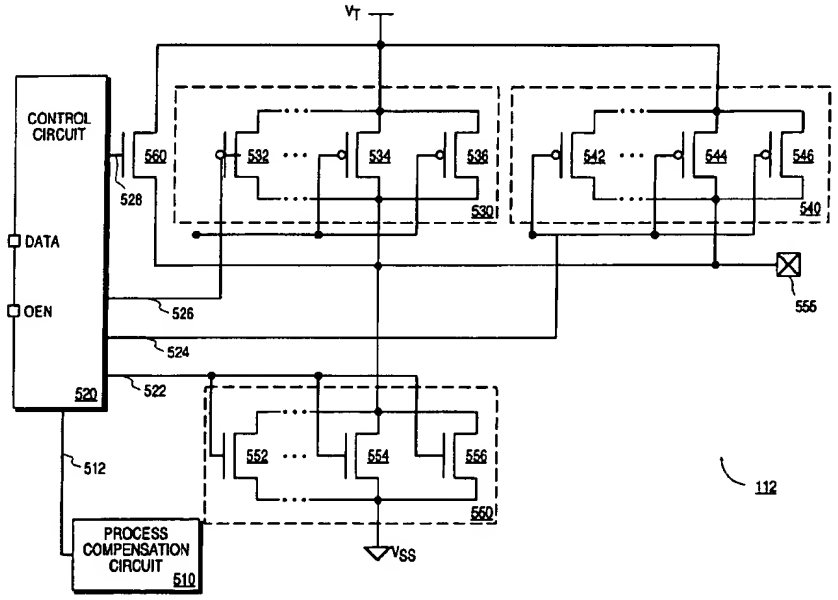
Primary Examiner—Paul R. Myers

Attorney, Agent, or Firm—Jeffrey S. Draeger

[57] ABSTRACT

A system utilizing distributed on-chip termination. The system comprises a bus having a signal line and a first bus agent which is coupled to the bus. The first bus agent has a first termination circuit which is coupled to selectably terminate the signal line to a termination voltage. The system may further comprise an additional bus agent. The additional bus agent has a second termination circuit coupled to selectably terminate the signal line to the termination voltage. The bus in the system has a bus impedance, and the impedance of the termination circuit(s) is typically greater than twice the bus impedance.

46 Claims, 5 Drawing Sheets



US005919252A

United States Patent [19]

Klein

[11] Patent Number: 5,919,252

[45] Date of Patent: Jul. 6, 1999

[54] **PROCESS AND APPARATUS FOR ADAPTIVE BUS TERMINATION**

[75] Inventor: **Dean A. Klein**, Lake City, Minn.

[73] Assignee: **Micron Electronics, Inc.**, Nampa, Id.

[21] Appl. No.: **08/977,640**

[22] Filed: **Nov. 24, 1997**

Related U.S. Application Data

[63] Continuation of application No. 08/012,020, Feb. 1, 1993, abandoned, which is a continuation of application No. 07/737,137, Jul. 29, 1991, abandoned.

[51] **Int. Cl.**[6] **G06F 13/00**

[52] **U.S. Cl.** **710/100**; 326/30

[58] **Field of Search** 326/30; 395/280, 395/281, 306, 309

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,220,876	9/1980	Ray	327/594
4,748,426	5/1988	Stewart	333/22 R
5,029,284	7/1991	Feldbaumer et al.	307/443
5,309,569	5/1994	Warchol	395/306
5,467,455	11/1995	Gay et al.	395/281

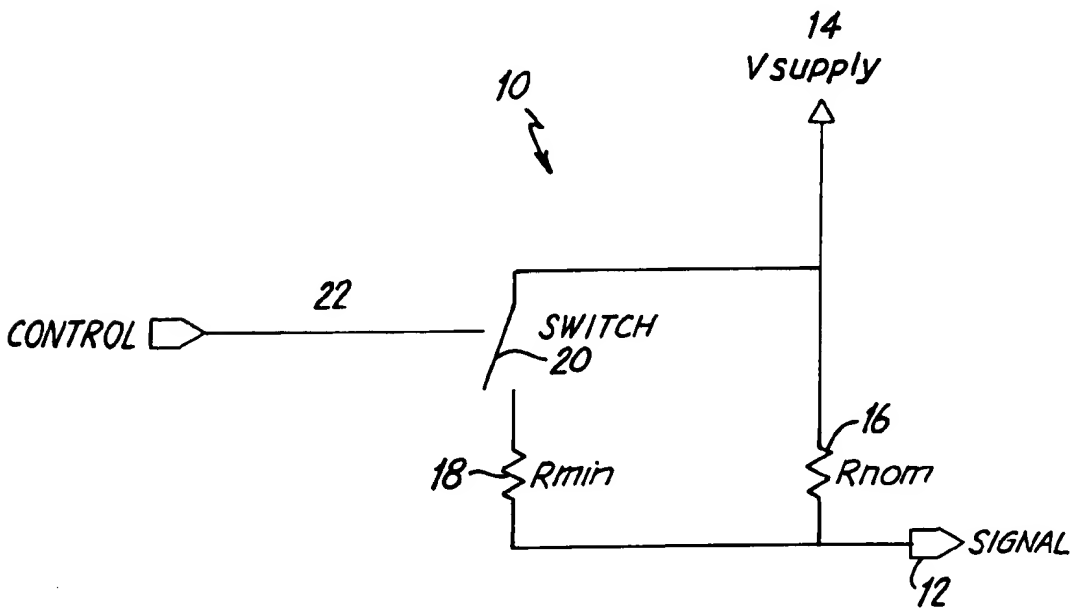
Primary Examiner—Glenn A. Auve

Attorney, Agent, or Firm—Dorsey & Whitney LLP

[57] **ABSTRACT**

Process and apparatus for reducing termination resistors on a CPU data bus and a CPU address bus. The reduced termination resistors are switched in, such as by a transistor switch or other switch, only during read operations when a CPU is receiving data from its bus or a CPU data bus only during hold acknowledge cycles. This increases the speed of the buses and allows the buses to be operation dependent. Further, power can be reduced during certain busing operations, resulting in cooler running and more reliable operations. Uses for adaptive termination includes microprocessor buses for data lines, address lines and control lines; peripheral devices for matching impedance to cable; and D/A converters. Variations on the device includes pull-up, pull-down, multiple levels/strengths, programmable with EPROM type cell, multiple units in the same package, and multiple values in the same package.

7 Claims, 5 Drawing Sheets



GENERIC ADAPTIVE SIGNAL PULL-UP

US005903736A

United States Patent [19]

Novak et al.

[11] Patent Number: 5,903,736

[45] Date of Patent: May 11, 1999

[54] METHOD AND APPARATUS FOR SMOOTH INDUCTIVE COMPENSATION OF TRANSMISSION BUS CAPACITIVE PARASITICS

[75] Inventors: Vit Frantisek Novak, Los Altos; Lawrence David Smith, San Jose, both of Calif.

[73] Assignee: Sun Microsystems, Inc., Palo Alto, Calif.

[21] Appl. No.: 08/831,369

[22] Filed: Apr. 1, 1997

[51] Int. Cl.[6] G06F 13/00; H03K 17/16

[52] U.S. Cl. 395/280; 326/30

[58] Field of Search 326/30, 86; 395/309, 395/287, 280, 285, 306

[56] References Cited

U.S. PATENT DOCUMENTS

5,528,167	6/1996	Samela et al.	326/30
5,553,250	9/1996	Miyagawa et al.	395/309
5,570,037	10/1996	Llorens	326/30

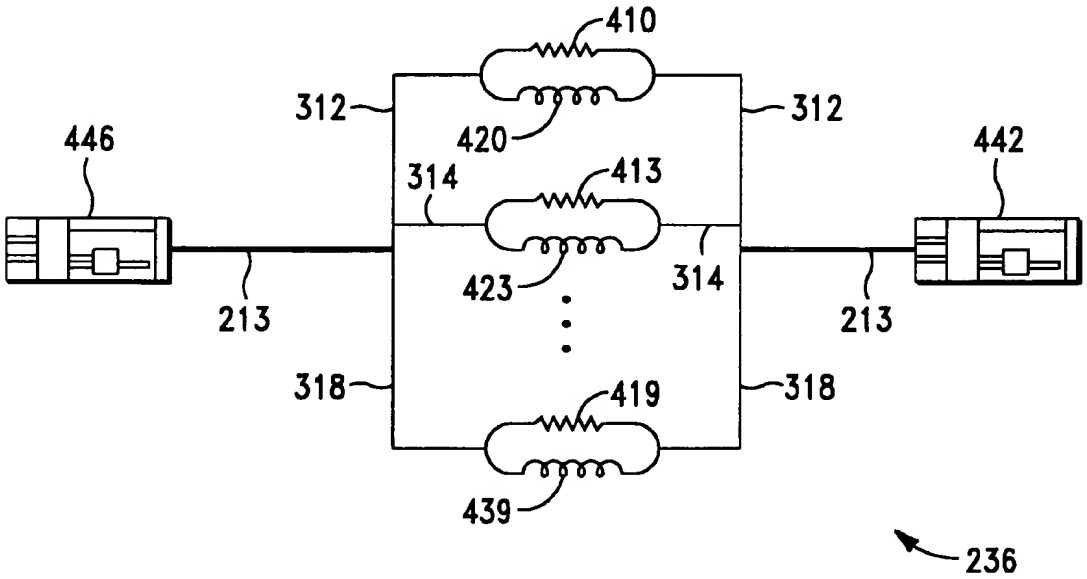
Primary Examiner—Glenn A. Auve

Attorney, Agent, or Firm—Peninsula Law Group; Daniel Hopen

[57] ABSTRACT

An inductive compensation apparatus for smooth compensation of a transmission bus and methods of operating the same result in improved impedance of the transmission bus for transfer of data signals. The inductive compensation apparatus having an input and an output and a transmission bus with an effective impedance comprises a first capacitance connected to the input and a second capacitance connected to the output. A first bus compensator is connected between the input and the first capacitance to compensate the first capacitance and raise the impedance of the transmission bus. A second bus compensator is connected between the first capacitance and the second capacitance to compensate the first capacitance and the second capacitance and raise the impedance of the transmission bus. A third bus compensator is connected between the second capacitance and the output to compensate the second capacitance and raise the impedance of the transmission bus for improved data transfers on the transmission bus.

20 Claims, 2 Drawing Sheets



US005864715A

United States Patent [19]

Zani et al.

[11] Patent Number: 5,864,715

[45] Date of Patent: Jan. 26, 1999

[54] **SYSTEM FOR AUTOMATICALLY TERMINATING A DAISY-CHAIN PERIPHERAL BUS WITH EITHER SINGLE-ENDED OR DIFFERENTIAL TERMINATION NETWORK DEPENDING ON PERIPHERAL BUS SIGNALS AND PERIPHERAL DEVICE INTERFACES**

[75] Inventors: **Mark Zani**, Derry, N.H.; **Charles Loewy**; **Thomas Georgens**, both of Upton, Mass.

[73] Assignee: **EMC Corporation**, Hopkinton, Mass.

[21] Appl. No.: **668,556**

[22] Filed: **Jun. 21, 1996**

[51] **Int. Cl.**[6] **G06F 13/10**; G06F 13/40

[52] **U.S. Cl.** **395/883**; 395/882; 395/280; 326/30

[58] **Field of Search** ..... 395/309, 500, 395/283, 750.06, 750.07, 883, 882, 280; 178/63 R; 307/147; 326/30

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,633,392	12/1986	Vincent et al.	395/284
4,864,291	9/1989	Korpi	340/825.5
5,099,137	3/1992	Lattin, Jr.	307/147
5,120,909	6/1992	Kutz et al.	178/63 R
5,220,286	6/1993	Nadeem	330/9
5,243,623	9/1993	Murdock	375/220
5,264,958	11/1993	Johnson	395/309
5,309,569	5/1994	Warchol	395/306
5,371,892	12/1994	Peterson et al.	395/651
5,379,405	1/1995	Ostrowski	395/500
5,381,034	1/1995	Thrower et al.	257/529
5,524,236	6/1996	Ostrowski	395/500
5,564,024	10/1996	Pemberton	395/283
5,596,757	1/1997	Smith	395/750.06
5,603,039	2/1997	Strevey	395/750.07
5,671,376	9/1997	Bucher et al.	395/309

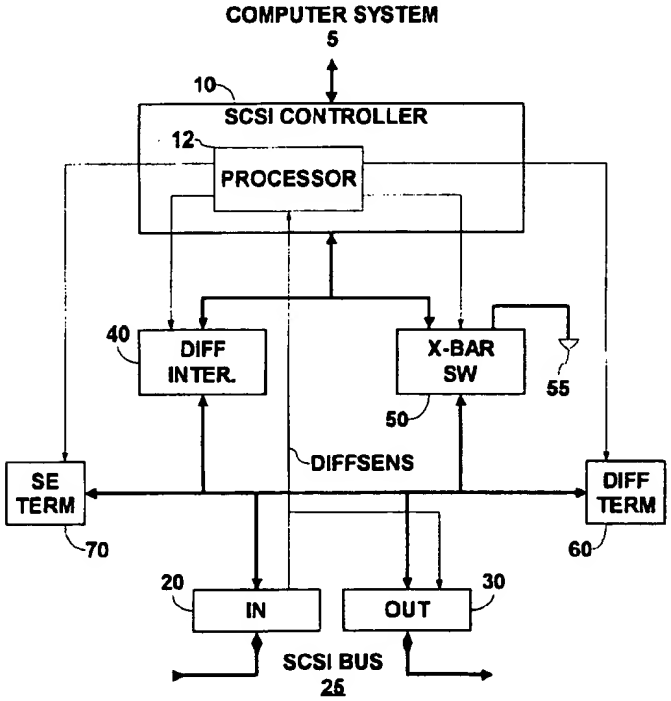
Primary Examiner—Le Hien Luu

Attorney, Agent, or Firm—David N. Caracappa

[57] **ABSTRACT**

A peripheral device interface is coupled between a computer system bus and a peripheral bus. The peripheral device bus includes a signal line which can be configured in either a single-ended or a differential configuration. A peripheral controller is coupled to the computer system bus. A single-ended signal line interface circuit is coupled between the peripheral bus signal line and the peripheral controller, and may be selectively enabled in response to a control signal. A differential signal line interface circuit is also coupled between the peripheral bus signal line and the peripheral controller and also may be selectively enabled in response to a control signal. The peripheral controller generates the control signals for the single-ended signal line interface circuit and the differential signal line interface circuit. Those control signals enable the single-ended signal line interface circuit when the peripheral bus signal line is a single-ended signal line and enable the differential signal line interface circuit when the peripheral bus signal line is a differential signal line.

11 Claims, 1 Drawing Sheet



US005634014A

United States Patent [19]

Gist et al.

[11] Patent Number: 5,634,014

[45] Date of Patent: May 27, 1997

[54] **SEMICONDUCTOR PROCESS, POWER SUPPLY VOLTAGE AND TEMPERATURE COMPENSATED INTEGRATED SYSTEM BUS TERMINATION**

[75] Inventors: **William B. Gist**, Chelmsford; **Joseph P. Coyle**, Leominster, both of Mass.

[73] Assignee: **Digital Equipment Corporation**, Maynard, Mass.

[21] Appl. No.: **501,388**

[22] Filed: **Jul. 12, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 79,515, Jun. 18, 1993, abandoned.

[51] **Int. Cl.**[6] **H04M 7/04**

[52] **U.S. Cl.** **395/280**; 326/30

[58] **Field of Search** 395/280; 307/443, 307/263, 270; 326/30

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,585,399	6/1971	Andrews	307/208
4,703,198	10/1987	Porter et al.	307/473
4,920,339	4/1990	Friend et al.	340/825.52
4,992,752	2/1991	Cioffi	330/54
5,029,284	7/1991	Feldbaumer et al.	307/443
5,049,836	9/1991	Christie et al.	330/277
5,095,231	3/1992	Satori et al.	307/475
5,134,311	7/1992	Biber et al.	307/270
5,185,538	2/1993	Kondoh et al.	307/270
5,187,454	2/1993	Collins et al.	333/17.3
5,202,649	4/1993	Kashiwa	333/33
5,294,845	3/1994	McMahan et al.	307/443
5,296,756	3/1994	Patel et al.	307/443
5,311,081	5/1994	Donaldson et al.	307/475
5,329,190	7/1994	Igarashi et al.	307/540
5,347,177	9/1994	Lipp	307/443
5,357,211	10/1994	Bryson et al.	330/263

OTHER PUBLICATIONS

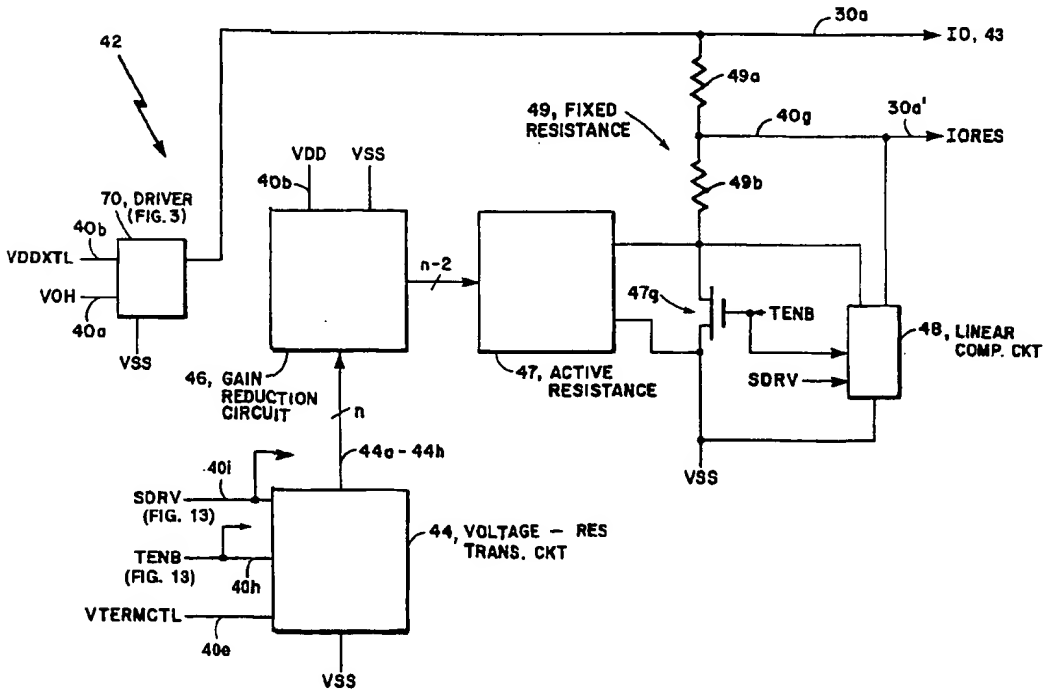
Electronics One-Seven, 1976 pp. 7-124.

Primary Examiner—Jack B. Harvey
Assistant Examiner—Paul R. Myers
Attorney, Agent, or Firm—Lindsay G. McGuinness; Denis G. Maloney; Arthur W. Fisher

[57] **ABSTRACT**

An I/O bus interface cell includes a driver circuit having an input terminal fed by a logic signal and an output terminal to produce in response thereto a drive signal having selectable rise and fall time characteristics in accordance with a reference voltage provided to the driver. The I/O cell also includes a receiver circuit having an input terminal coupled to said output terminal of said driver with the receiver disposed to latch an unresolved, unamplified received signal prior to resolving the state of the signal. The I/O cell further includes a termination circuit having a terminal connected to the output of said driver, and having a selectable impedance characteristic at said terminal, with said selectable impedance being in accordance with a reference voltage provided to an input of said termination circuit. Preferably, the I/O cell the driver, receiver and termination circuits are fabricated on a common semiconductor substrate.

10 Claims, 23 Drawing Sheets



US005613074A

United States Patent [19]

Galloway

[11] Patent Number: 5,613,074

[45] Date of Patent: Mar. 18, 1997

[54] **AUTOMATIC DISABLING OF SCSI BUS TERMINATORS**

[75] Inventor: **William C. Galloway**, Houston, Tex.

[73] Assignee: **Compaq Computer Corporation**, Houston, Tex.

[21] Appl. No.: **366,510**

[22] Filed: **Dec. 30, 1994**

[51] **Int. Cl.**[6] **H01J 13/00**

[52] **U.S. Cl.** **395/280**; 395/281; 395/821; 395/835; 395/287; 395/306; 395/308; 326/30

[58] **Field of Search** 395/281, 287, 395/282, 306, 307, 308, 283, 284, 309; 326/30

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 33,521	1/1991	Mori et al. .	
4,320,508	3/1982	Takezoe .	
4,402,082	8/1983	Cope .	
4,920,339	4/1990	Friend et al. .	
5,033,049	7/1991	Keener et al. .	
5,120,909	6/1992	Kutz et al. .	
5,272,396	12/1993	Mammano et al. .	
5,309,569	5/1994	Warchol .	
5,313,595	5/1994	Lewis et al. .	
5,338,979	8/1994	Mammano et al. .	
5,357,519	10/1994	Martin et al. .	
5,434,516	7/1995	Kosco	326/30
5,467,453	11/1995	Kocis	395/281

FOREIGN PATENT DOCUMENTS

3016445	4/1991	Japan .
3023706	4/1991	Japan .
4-247742	9/1992	Japan .
2168574	6/1986	United Kingdom .

OTHER PUBLICATIONS

X3T10/1071D draft proposed American National Standard for Information Systems—SCSI-3 Fast-20, revision 6 (Oct., 1994).

X3T10/855D draft proposed American National Standard Information Technology—SCSI-3 Parallel Interface, revision 15a (Feb., 1992).

Unitrode Integrated Circuits 9-Line SCSI Activer Terminator (UC5603), Sep. 1994.

Unitrode Integrated Circuits SCSI Activer Terminator (UC5601), Sep. 1994.

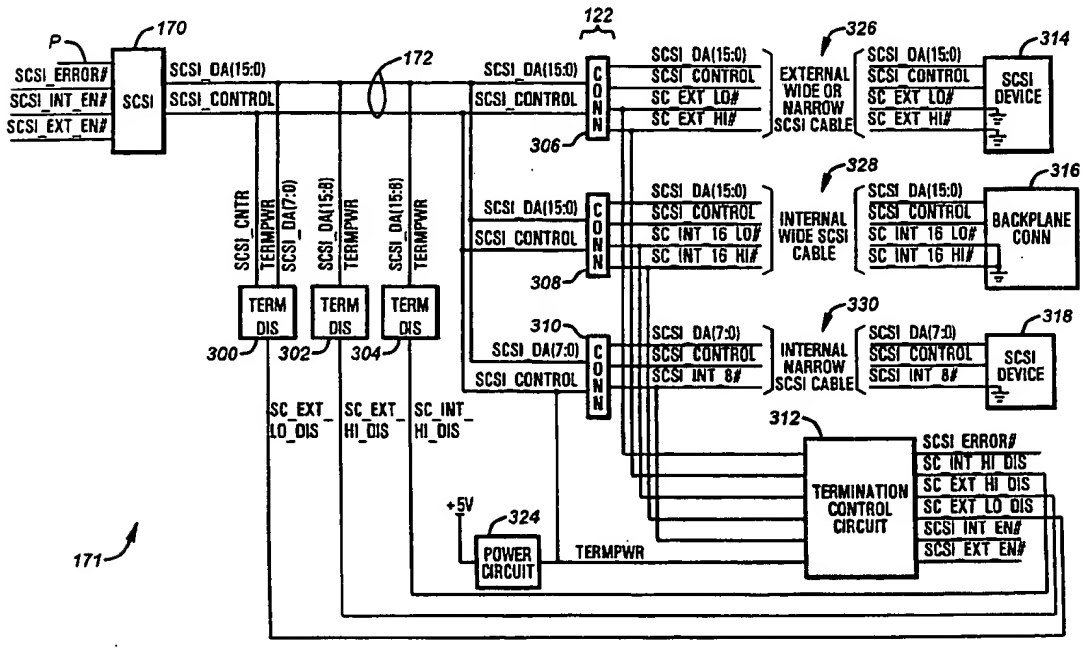
Notebook—Small Computer System Interface—2, Working Draft, X3T9.2 Project 375D, printed Sep. 7, 1993.

Primary Examiner—Jack B. Harvey
Assistant Examiner—Raymond N. Phan
Attorney, Agent, or Firm—Pravel, Hewitt, Kimball & Krieger

[57] **ABSTRACT**

A system for detecting the presence and size of a SCSI device on a SCSI bus and terminating the SCSI bus accordingly. A SCSI controller is capable of driving two branches of a SCSI bus, each branch having a different data size. When the SCSI controller is at the end of a SCSI chain, termination is enabled, otherwise termination is disabled. Termination is performed on the portions of the SCSI data bus requiring termination based on the presence and size of SCSI devices on the branches used.

19 Claims, 7 Drawing Sheets



US005596757A

United States Patent [19]

Smith

[11] Patent Number: 5,596,757

[45] Date of Patent: Jan. 21, 1997

[54] **SYSTEM AND METHOD FOR SELECTIVELY PROVIDING TERMINATION POWER TO A SCSI BUS TERMINATOR FROM A HOST DEVICE**

[75] Inventor: **Mark L. Smith**, Laguna Beach, Calif.

[73] Assignee: **Simple Technology, Inc.**, Santa Ana, Calif.

[21] Appl. No.: **390,749**

[22] Filed: **Feb. 16, 1995**

[51] **Int. Cl.**[6] **G06F 1/26**; G06F 1/32

[52] **U.S. Cl.** **395/750**; 395/281; 395/822; 326/30; 333/32

[58] **Field of Search** 326/30; 395/306, 395/281, 750

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,204,249	5/1980	Dye et al.	395/750
4,312,035	1/1982	Greene	395/750
4,316,246	2/1982	Hartley et al.	395/750
4,575,759	3/1986	Griepentrog et al.	348/706
4,631,721	12/1986	Ono et al.	370/85.9
4,920,339	4/1990	Friend et al.	340/825.52
5,029,284	7/1991	Feldbaumer et al.	326/30
5,099,137	3/1992	Lattin, Jr.	307/147
5,120,909	6/1992	Kutz et al.	326/30
5,157,769	10/1992	Eppley et al.	395/200.01
5,163,124	11/1992	Yabe et al.	395/750
5,239,559	8/1993	Brach et al.	375/257
5,239,652	8/1993	Seibert et al.	395/750
5,239,658	8/1993	Yamamuro et al.	395/800
5,272,396	12/1993	Mammano et al.	307/443
5,309,569	5/1994	Warchol	395/306
5,313,105	5/1994	Samela et al.	307/99
5,313,595	5/1994	Lewis et al.	395/306
5,327,172	7/1994	Tan et al.	348/378
5,369,771	11/1994	Gettel	395/750
5,404,542	4/1995	Cheung	395/750
5,422,580	6/1995	Mandel et al.	326/30
5,450,003	9/1995	Cheon	323/272
5,467,453	11/1995	Kocis	395/281
5,467,455	11/1995	Gay et al.	395/281
5,513,373	4/1996	Damkier	395/836

OTHER PUBLICATIONS

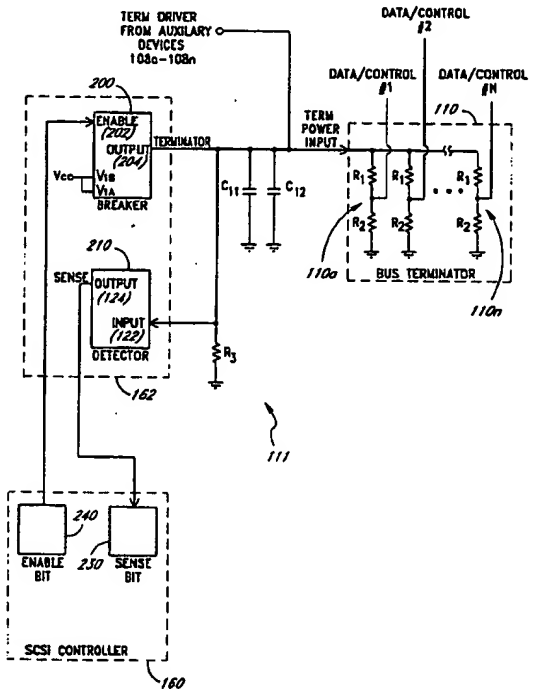
PCMCIA Cards Data Sheets, STI–SCSI, Simple Technology, Nov. 1994.

Primary Examiner—Jack B. Harvey
Assistant Examiner—Sumati Lefkowitz
Attorney, Agent, or Firm—Knobbe Martens Olson & Bear

[57] **ABSTRACT**

A system which determines whether one of a plurality of peripheral devices on a SCSI bus is providing termination power to a bus terminator and provides termination power from a power supply associated with a host device only when none of the peripheral devices are providing termination power. The system is further configured to only provide termination power from the host device when information signals are likely to be present on the information bus. Specifically, the system only provides termination power when the host device seeks access to the information bus to thereby limit consumption of the host device's power supply.

30 Claims, 4 Drawing Sheets



US005553250A

United States Patent [19]

Miyagawa et al.

[11] Patent Number: 5,553,250

[45] Date of Patent: Sep. 3, 1996

[54] **BUS TERMINATING CIRCUIT**

[75] Inventors: **Takao Miyagawa; Akinori Kashio; Ken Hashimoto; Makoto Yasuda; Hidenobu Sakai; William C. Kutsche,** all of Nagaokakyo, Japan

[73] Assignee: **Murata Manufacturing Co., Ltd.,** Japan

[21] Appl. No.: **281,259**

[22] Filed: **Jul. 27, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 109,402, Aug. 19, 1993, abandoned, which is a continuation of Ser. No. 811,708, Dec. 20, 1991, abandoned.

[30] **Foreign Application Priority Data**

Dec. 20, 1990	[JP]	Japan	2-413559
Mar. 1, 1991	[JP]	Japan	3-061174
Jul. 19, 1991	[JP]	Japan	3-204948
Sep. 5, 1991	[JP]	Japan	3-254499
Oct. 11, 1991	[JP]	Japan	3-292154
Dec. 10, 1991	[JP]	Japan	3-350890

[51] **Int. Cl.**[6] **G06F 13/40**

[52] **U.S. Cl.** **395/309**; 326/30; 326/86

[58] **Field of Search** 395/325, 725, 395/275, 200, 280, 309, 310, 306; 326/30, 86, 90

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,220,876	9/1980	Ray	327/594
4,674,085	6/1987	Aranguren	370/85.2
4,748,426	5/1988	Stewart	333/22 R
4,920,339	4/1990	Friend	340/825.52
5,029,284	7/1991	Feldbaumer	326/30
5,101,153	3/1992	Morong	324/537
5,239,658	8/1993	Yamamuro et al.	395/800
5,272,396	12/1993	Mammano et al.	326/21
5,309,569	5/1994	Warchol	395/306
5,313,595	5/1994	Lewis et al.	395/306
5,367,647	11/1994	Coulson et al.	395/285

OTHER PUBLICATIONS

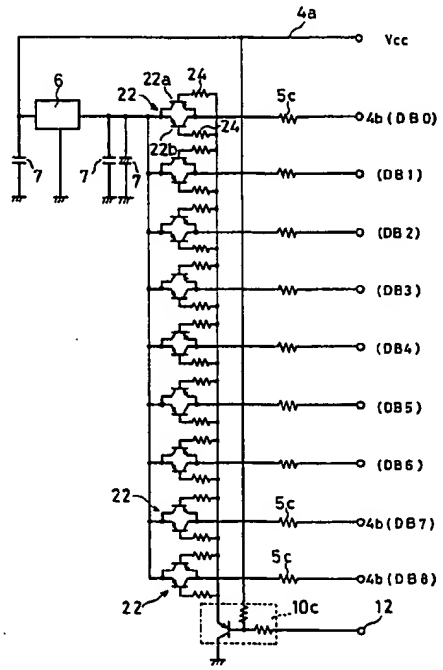
Microelectronic Circuits; Sedra, Adel and Smith, Kenneth; Holt, Rinehart and Winston; 1982; p. 509.

Primary Examiner—Jack B. Harvey
Assistant Examiner—Glenn A. Auve
Attorney, Agent, or Firm—Ostrolenk, Faber, Gerb & Soffen, LLP

[57] **ABSTRACT**

A bus terminating circuit is provided on each of a plurality of SCSI devices connected to each other through an SCSI bus line. A first terminating resistor is inserted between each of the signal lines and a power source line of the bus line and a second terminating resistor is inserted between each of the signal lines and ground. A first transistor is connected between the first terminating resistor and the power source line and a second transistor is connected between the second terminating resistor and ground. The first and second transistors are turned-on or off in response to an ON signal or an OFF signal inputted from an external terminal so that the first and second resistors can be connected or disconnected to or from the bus line.

20 Claims, 15 Drawing Sheets



US005495584A

United States Patent [19]

Holman, Jr. et al.

[11] Patent Number: 5,495,584

[45] Date of Patent: Feb. 27, 1996

[54] **SCSI BUS CONCATENATOR/SPLITTER**

[75] Inventors: **Thomas H. Holman, Jr.; Peter D. Geiger**, both of Austin, Tex.

[73] Assignee: **Dell USA, L.P.**, Austin, Tex.

[21] Appl. No.: **28,506**

[22] Filed: **Mar. 9, 1993**

[51] **Int. Cl.**[6] **G06F 13/00**; H03H 11/28; H04B 3/00

[52] **U.S. Cl.** **395/308**; 395/280; 340/825.06; 326/30; 370/53; 364/240.2; 364/239.9; 364/240; 364/DIG. 1

[58] **Field of Search** 395/325, 275, 395/425, 308, 280; 340/825.5, 825.06; 370/85.1, 53; 326/30

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,245,301	1/1981	Rokutanda et al.	395/325
4,422,142	12/1983	Inaba et al.	395/325
4,812,840	3/1989	Girard	340/840.5
4,814,977	3/1989	Buonomo et al.	395/425
4,821,170	4/1989	Bernick et al.	395/275
4,975,838	12/1990	Mizuno et al.	395/275
4,984,195	1/1991	Nakamura et al.	395/325
5,083,259	1/1992	Maresh et al.	395/325
5,202,980	4/1993	Morita et al.	395/575
5,305,317	4/1994	Szezepanek	370/85.5
5,313,595	5/1994	Lewis et al.	395/325
5,369,748	11/1994	McFarland et al.	395/325
5,422,580	6/1995	Mandel et al.	326/30

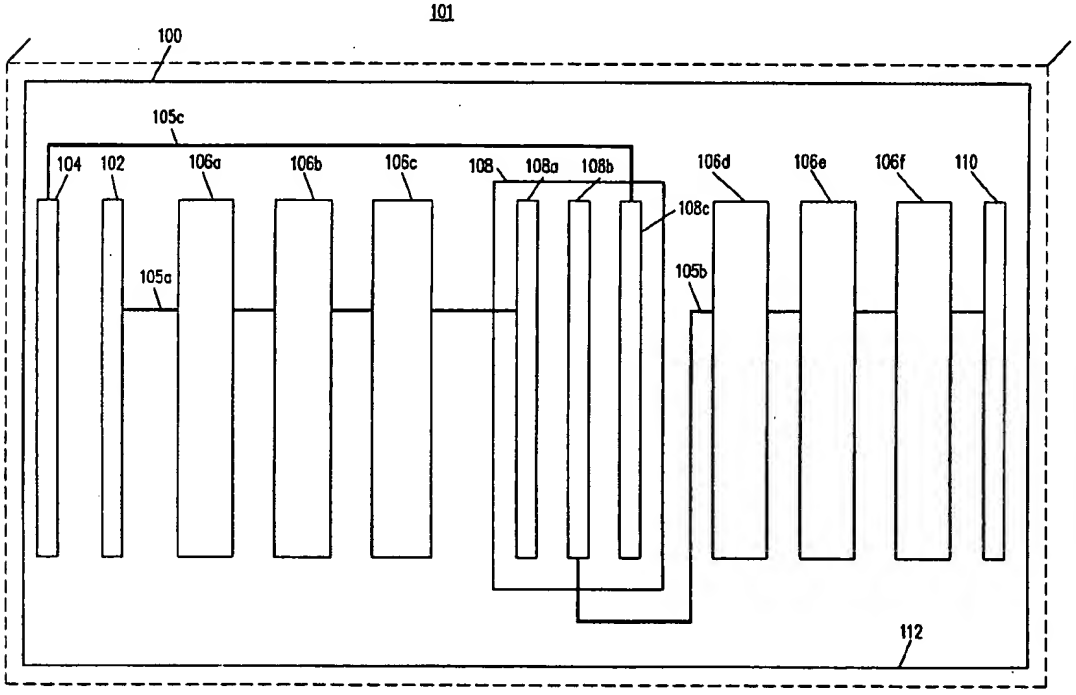
Primary Examiner—Gopal C. Ray

Attorney, Agent, or Firm—James W. Huffman; David L. McCombs

[57] **ABSTRACT**

A system is described for selectively configuring a backplane-based SCSI subsystem in at least two alternative drive configurations. A concatenator/splitter (C/S) device enables a user to concatenate several SCSI devices onto a single bus, or alternatively to split the devices onto multiple buses. In either configuration, the bus or buses are properly terminated. The C/S device is located on the backplane between two buses and is connected to each bus by a connector section. A removable interface module plugs into the connector section in either an upright or upside-down orientation, as selected by the user, to choose either a concatenated or split bus configuration. A terminating network is included in the interface module in order to terminate the first bus when the subsystem is configured in the split bus arrangement.

15 Claims, 2 Drawing Sheets



US005495584A

United States Patent [19]

Holman, Jr. et al.

[11] Patent Number: 5,495,584

[45] Date of Patent: Feb. 27, 1996

[54] **SCSI BUS CONCATENATOR/SPLITTER**

[75] Inventors: **Thomas H. Holman, Jr.; Peter D. Geiger**, both of Austin, Tex.

[73] Assignee: **Dell USA, L.P.**, Austin, Tex.

[21] Appl. No.: **28,506**

[22] Filed: **Mar. 9, 1993**

[51] **Int. Cl.**[6] **G06F 13/00**; H03H 11/28; H04B 3/00

[52] **U.S. Cl.** **395/308**; 395/280; 340/825.06; 326/30; 370/53; 364/240.2; 364/239.9; 364/240; 364/DIG. 1

[58] **Field of Search** 395/325, 275, 395/425, 308, 280; 340/825.5, 825.06; 370/85.1, 53; 326/30

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,245,301	1/1981	Rokutanda et al.	395/325
4,422,142	12/1983	Inaba et al.	395/325
4,812,840	3/1989	Girard	340/840.5
4,814,977	3/1989	Buonomo et al.	395/425
4,821,170	4/1989	Bernick et al.	395/275
4,975,838	12/1990	Mizuno et al.	395/275
4,984,195	1/1991	Nakamura et al.	395/325
5,083,259	1/1992	Maresh et al.	395/325
5,202,980	4/1993	Morita et al.	395/575
5,305,317	4/1994	Szezepanek	370/85.5
5,313,595	5/1994	Lewis et al.	395/325
5,369,748	11/1994	McFarland et al.	395/325
5,422,580	6/1995	Mandel et al.	326/30

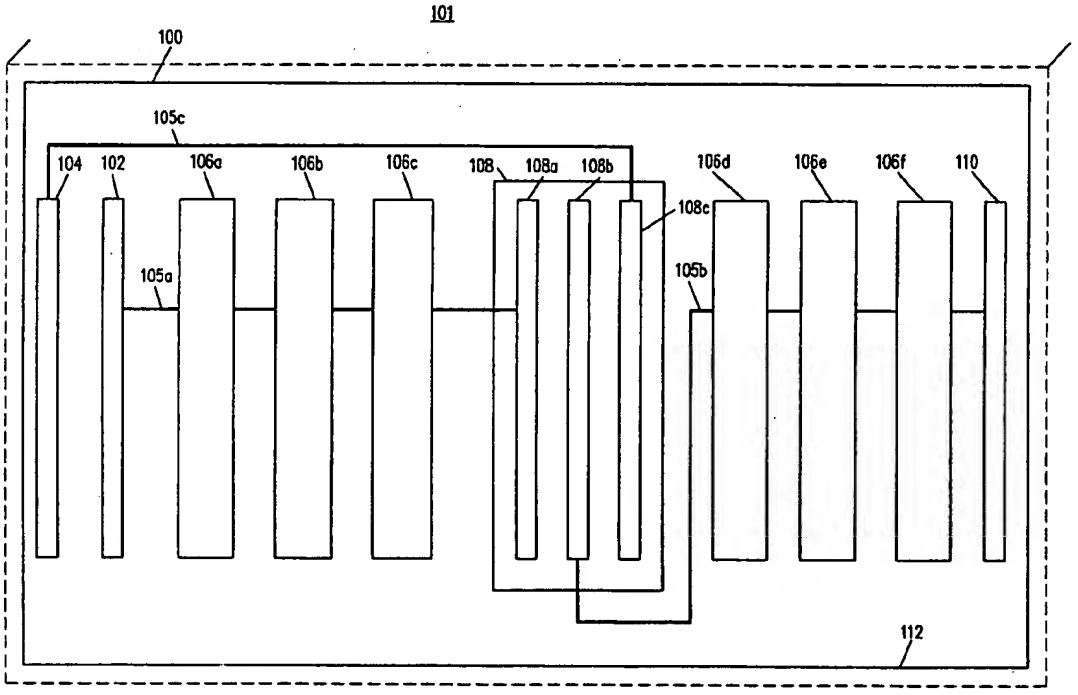
Primary Examiner—Gopal C. Ray

Attorney, Agent, or Firm—James W. Huffman; David L. McCombs

[57] **ABSTRACT**

A system is described for selectively configuring a backplane-based SCSI subsystem in at least two alternative drive configurations. A concatenator/splitter (C/S) device enables a user to concatenate several SCSI devices onto a single bus, or alternatively to split the devices onto multiple buses. In either configuration, the bus or buses are properly terminated. The C/S device is located on the backplane between two buses and is connected to each bus by a connector section. A removable interface module plugs into the connector section in either an upright or upside-down orientation, as selected by the user, to choose either a concatenated or split bus configuration. A terminating network is included in the interface module in order to terminate the first bus when the subsystem is configured in the split bus arrangement.

15 Claims, 2 Drawing Sheets



US005467455A

United States Patent [19]

Gay et al.

[11] Patent Number: 5,467,455

[45] Date of Patent: Nov. 14, 1995

[54] **DATA PROCESSING SYSTEM AND METHOD FOR PERFORMING DYNAMIC BUS TERMINATION**

[75] Inventors: **James G. Gay**, Pflugerville; **William B. Ledbetter, Jr.**, Austin, both of Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **145,117**

[22] Filed: **Nov. 3, 1993**

[51] **Int. Cl.**[6] **G01R 27/00**; H03H 7/40

[52] **U.S. Cl.** **395/281**; 333/32; 333/17.3; 395/822

[58] **Field of Search** ..... 395/325; 333/17.3, 333/22 R, 32

[56] **References Cited**

U.S. PATENT DOCUMENTS

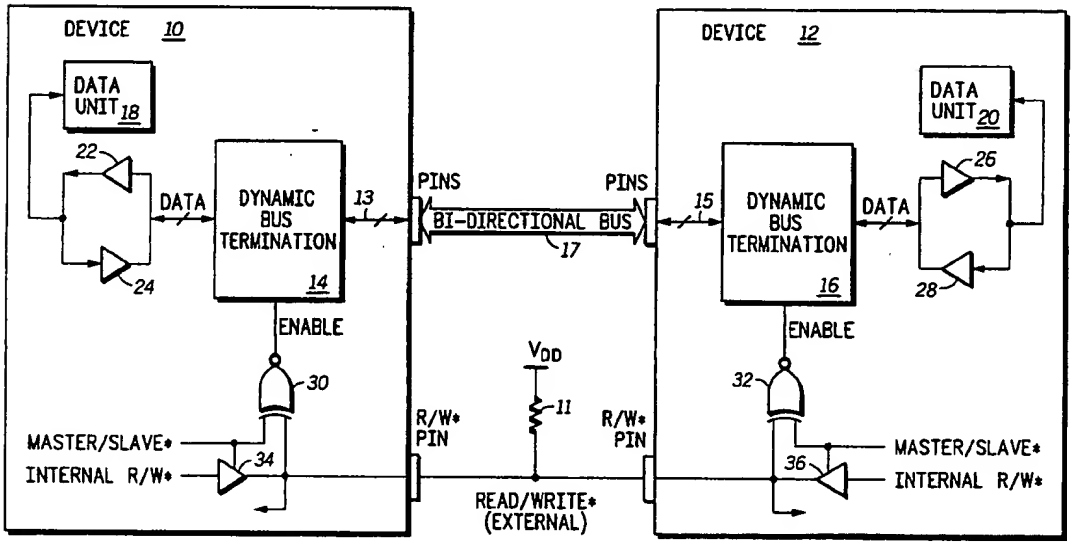
3,435,375	3/1969	Miller	331/110
3,854,057	12/1974	Williams et al.	330/17.13
4,567,385	1/1986	Falater et al.	307/443
4,695,740	9/1987	Carter	307/242
4,761,647	8/1988	Hallenbeck et al.	340/825.22
4,791,322	12/1988	Graham et al.	307/475
4,806,802	2/1989	Okitaka et al.	307/542
4,839,537	6/1989	Ueno	307/446
4,853,560	8/1989	Iwamura et al.	307/296.1
4,877,978	10/1989	Platt	307/473
4,975,598	12/1990	Borkar	307/443
5,039,874	8/1991	Anderson	307/270
5,057,783	10/1991	Gubisch	324/710
5,059,830	10/1991	Tokumaru et al.	307/481
5,063,308	11/1991	Borkar	307/443
5,162,672	11/1992	McMahan et al.	307/443
5,294,845	3/1994	McMahan et al.	307/443

Primary Examiner—Jack B. Harvey
Assistant Examiner—Jeffrey K. Seto
Attorney, Agent, or Firm—Keith E. Witek

[57] **ABSTRACT**

A data processing system and a method for performing dynamic bus signal termination uses a dynamic bus termination circuitry (**14** or **16**) with a device (**10** or **12**). The circuitry is enabled when data is incoming to the device and is disabled when data is outgoing from the device to selectively reduce unwanted signal reflection at the signal end of a bi-directional bus (**17**). The disabling allows the circuitry to be removed or tristated from any connection with the bus (**17**) when not needed (i.e., data outgoing) to reduce loading. The disabling of the termination circuitry also aids in reducing the power consumption of the part when either the bus is sitting idle or the part is in a low power mode of operation.

29 Claims, 7 Drawing Sheets



US-CL-CURRENT: 326/30,333/17.3 ,333/32 ,710/2

US-PAT-NO: 5467455
DOCUMENT-IDENTIFIER: US 5467455 A
TITLE: Data processing system and method for performing dynamic bus termination
DATE-ISSUED: November 14, 1995
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gay; James G.	Pflugerville	TX	N/A	N/A
Ledbetter, Jr.; William B.	Austin	TX	N/A	N/A

US-CL-CURRENT: 710/100,326/30 ,333/17.3 ,333/32 ,710/2
ABSTRACT:
A data processing system and a method for performing dynamic bus signal termination uses a dynamic bus termination circuitry (14 or 16) with a device (10 or 12). The circuitry is enabled when data is incoming to the device and is disabled when data is outgoing from the device to selectively reduce unwanted signal reflection at the signal end of a bi-directional bus (17). The disabling allows the circuitry to be removed or tristated from any connection with the bus (17) when not needed (i.e., data outgoing) to reduce loading. The disabling of the termination circuitry also aids in reducing the power consumption of the part when either the bus is sitting idle or the part is in a low power mode of operation.
29 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

CCOR:
710/100

CCXR:
326/30

US-CL-CURRENT: 257/701

US-PAT-NO: 6310392
DOCUMENT-IDENTIFIER: US 6310392 B1
TITLE: Stacked micro ball grid array packages
DATE-ISSUED: October 30, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Burns; Carmen D.	Austin	TX	N/A	N/A

US-CL-CURRENT: 257/723,257/701
ABSTRACT:

Integrated circuit modules made in accordance with the methods of the present invention have multiple Ball-Grid Array (BGA) packages mounted to a substantially planar support substrate. Each package is inclined at an angle to the support substrate and partially overlaps another package. The first package or row of packages overlaps a wedge that is provided for support. A flexible substrate is mounted to each BGA package and has a portion that extends away from the package to adhere to the support substrate, for communication between each package and signal lines on the support substrate. Optionally, a portion of the substrate that extends away from the integrated circuit package can be bent back at a 180.degree. angle to allow the pads on the top surface of the flexible substrate to attach to mating pads on the support substrate. Precise control of the impedance of select signal traces is
accomplished through the use of ground traces that run parallel with the select
signal, a ground plane layer, and alternating signal-substrate mounting pads with GND-substrate mounting pads. One aspect of the present invention has the package leads located in close proximity to one side of the package for optimally short trace lengths. Another aspect provides a method for routing signals for optimal signal length and elimination of stubs. A preferred embodiment of a flexible substrate has an accordion portion formed in the flexible substrate to provide elasticity for preventing stretching and distortions of the flexible substrate during automated assembly. A method is provided for connecting signals lines of each flexible substrate in series. Various embodiments of package lead mounting pads formed in the flexible substrate that provide electrical and thermal coupling to package leads including ring-shaped pads, flexible tabs, and apertures for removing flux, excess solder, and debris.
17 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 9

BSPR:
DIMMs based on RAMBUS.TM. technology are capable of data transfer rates up to 800 Mhz using low voltage swings of 800 mv. Data is transferred across a 16-bit bus on both edges of a 400 Mhz-clock signal. The high-speed operation of a RAMBUS CHANNEL.TM. requires dense packaging and high quality transmission
lines. The RAMBUS CHANNEL.TM. high-speed signals require matched transmission
lines that have the identical propagation characteristics and travel across a uniform, parallel layout. These high-speed signals require a uniform matched impedance of **25 to 65 ohms** over the entire length of each signal-transmission line after all components are installed. Multiple DRAM components that are electrically coupled to a single data transmission line present periodically

spaced capacitive loads, which significantly effect the impedance of a portion of the transmission line. The periodic spacing between these capacitive loads on the transmission line is referred to as pitch. Decreasing the pitch has the
effect of decreasing the impedance of the transmission line as a whole. Other parameters which effect the impedance of a signal transmission line are the properties and thickness of the material located between the line and either an
adjacent ground plane, ground line, or signal line. Increasing the dielectric thickness or decreasing the signal line width has the effect of increasing the impedance of the effected portion of the transmission line. RAMBUS.TM. layout
guidelines require the high-speed channel signals to be routed on a single signal layer with no vias, and with data signals routed in parallel with clock signals. Vias typically have a physical shape that creates a capacitance effect in the order of 1 pF; for this reason, the RAMBUS CHANNEL.TM. guidelines state that vias are not allowed on high-speed transmission lines. These guidelines allow for 20% variation in dielectric thickness, signal line trace widths, and copper thickness. Signal line trace length among the 13 high-speed signals can vary by 100 mils (2.5 mm). Deviations from the guidelines that maintain the desired transmission line characteristics are acceptable.

US-CL-CURRENT: 327/308

US-PAT-NO: 4378536
DOCUMENT-IDENTIFIER: US 4378536 A
TITLE: High power, low frequency, electronically adjustable attenuator
DATE-ISSUED: March 29, 1983
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Schwarzmann; Alfred	Mount Laurel	NJ	N/A	N/A

US-CL-CURRENT: 333/81R,327/308
ABSTRACT:

An attenuator for high-power, low frequency RF signals including two .pi.-section low-pass filters is well matched to the transmission line characteristic impedance. Each of the four loss branches of the attenuator includes a power resistor and a PIN diode. The attenuator is made electronically variable by controlling the dc bias across the PIN diodes, which respond to increased voltage by exhibiting lowered resistance. At any setting of the dc bias, only a fraction of the attenuated RF power is dissipated by the diodes. When the bias voltage is tuned for high attenuation, virtually all of the power is dissipated by the power resistors.

3 Claims, 2 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

DEPR:
The useful attenuation range of the attenuator constructed using 100 ohms as the value of resistors 19, 21, 23, and 25 is one to six db. A greater power handling capacity can be obtained by increasing the values of resistors 19, 21, 23, and 25 to 150 ohms, at the sacrifice of a decreased attenuation range of one to four db. If an increased attenuation range is required, a useful range of one to ten db can be provided at a sacrifice of power handling capacity, by the selection of **65 ohms for resistors 19 and 25 and 30 ohms** for resistors 21 and 23.

L Number	Hits	Search Text	DB	Time stamp
1	739	326/30.ccls.	USPAT; US-PGPUB	2001/11/28 10:51
4	698	710/100.ccls.	USPAT; US-PGPUB	2001/11/28 10:52
7	16	326/30.ccls. and 710/100.ccls.	USPAT; US-PGPUB	2001/11/28 11:00
10	213545	resistor$1	USPAT; US-PGPUB	2001/11/28 11:10
13	26251	25$ with 65$	USPAT; US-PGPUB	2001/11/28 11:14
14	0	("25" adj ohms) near5 ("65" adj ohms)	USPAT; US-PGPUB	2001/11/28 11:15
17	2	("25" adj2 ohms) near5 ("65" adj2 ohms)	USPAT; US-PGPUB	2001/11/28 11:20
20	0	("25" adj2 ohms) near5 ("65" adj2 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:20
25	0	("25" adj3 ohms) near10 ("65" adj3 ohms)	EPO; JPO; DERWENT; IBM TDB	2001/11/28 11:20
30	6	("25" adj3 ohms) near10 ("65" adj3 ohms)	USPAT; US-PGPUB	2001/11/28 11:21

US-CL-CURRENT: 326/30,326/86 ,326/93

US-PAT-NO: 6266730
DOCUMENT-IDENTIFIER: US 6266730 B1
TITLE: High-frequency bus system
DATE-ISSUED: July 24, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Perino; Donald V.	Los Altos	CA	N/A	N/A
Garrett, Jr.; Billy	Mountain View	CA	N/A	N/A
Wayne	Sunnyvale	CA	N/A	N/A
Liaw; Haw-Jyh	San Jose	CA	N/A	N/A
Nguyen; David	Santa Clara	CA	N/A	N/A
Nimmagadda; Srinivas	Mountain View	CA	N/A	N/A
Gasbarro; James A.	San Jose	CA	N/A	N/A
Crisp; Richard DeWitt				

US-CL-CURRENT: 710/300,326/30 ,326/86 ,326/93
ABSTRACT:
A high frequency bus system which insures uniform arrival times of high-fidelity signals to the devices on the high frequency bus, despite the use of the bus on modules and connectors. A high frequency bus system includes a first bus segment having one or more devices connected between a first and a second end. The first bus segment has at least a pair of transmission lines for propagating high frequency signals and the devices are coupled to the pair of transmission lines. The high frequency bus system also includes a second bus segment which has no devices connected to it. The second bus segment also has at least a pair of transmission lines for propagating high frequency signals. The first end of the first segment and second end of the second segment are coupled in series to form a chain of segments and when two signals are introduced to the first end of the second bus segment at the substantially the same time, they arrive at each device connected to the first bus segment at substantially the same time. Also, when two signals originate at a device connected to the first bus segment at substantially the same time, they arrive at the first end of the second bus segment at substantially the same time. Uniform arrival times hold despite the use of connectors to couple the segments together, despite the segments being located on modules, without the need for stubs, despite the presence of routing turns in the segments and despite the type of information, such as address, data or control, carried by the signals.
20 Claims, 26 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 21

BSPR:
A circuit model of a tapped line, typical of the second group of lines, is shown in FIG. 3. As shown, in this topology, each line in a group is typically connected to a module by means of a stub 360 which acts as tap off of the line as shown in FIG. 2 and FIG. 3. A stub is defined as a length of line tapped from a transmission line and having a round trip delay which is greater than the rise time (or fall time) of the signal. Since the stub 360 (160 in FIG. 2) typically has a different impedance than the line being tapped, it is often necessary to insert a **resistor** 320, as shown in FIG. 3, in series with the

stub
to mitigate the effect of reflections at the connection point of the stub to the line. If the line impedance is **about 50 ohms and the impedance of the stub**
is about 75 ohms, a **resistor** of approximately 20-25 ohms is typically chosen usually by trial and error for the best results under certain conditions. This
resistor has the possibly undesirable effect of attenuating the voltage swing of the signal as the signal passes through the **resistor,** requiring a driver on the stub to have a proportionately larger voltage swing. Another undesirable effect is the RC delay due to the added series **resistor** and the device capacitance. The **resistors** and stubs also lead to low-fidelity signals at the devices. Also, as shown in FIG. 3, the **line is terminated by resistors** 350 at both ends to minimize reflections from the ends of the **line**. This requires that the drivers on the **line** supply twice as much steady state current as compared to a **line terminated** at only one end.

US-CL-CURRENT: 174/255,257/533 ,257/536 ,257/537 ,257/780 ,338/330 ,338/331 ,338/333 ,361/765 ,361/766 ,361/767 ,361/772 ,361/782 ,361/783

US-PAT-NO: 6108212
DOCUMENT-IDENTIFIER: US 6108212 A
TITLE: Surface-mount device package having an integral passive component
DATE-ISSUED: August 22, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lach; Lawrence E.	Chicago	IL	N/A	N/A
Dunn; Gregory J.	Arlington Heights	IL	N/A	N/A
Gamota; Daniel R.	Palatine	IL	N/A	N/A

US-CL-CURRENT: 361/768,174/255 ,257/533 ,257/536 ,257/537 ,257/780 ,338/330 ,338/331 ,338/333 ,361/765 ,361/766 ,361/767 ,361/772 ,361/782 ,361/783
ABSTRACT:

The surface-mount device package comprises a pad located on a face of the surface-mount device, a solder bump bonded to the pad, and a terminal spaced radially apart from the pad. A terminal surrounds the pad in at least one common plane that bisects the pad and the terminal. An electrically resistive volume intervenes between the pad and the terminal. The pad is electrically coupled to the terminal through the resistive volume. The terminal, the pad, and the electrically resistive volume cooperate to form a passive component associated with at least one device interconnection. The passive component preferable comprises an integral resistor. The integral resistor serves to eliminate or at least substantially reduce electrical resonances and reflections that may otherwise degrade the signal integrity.

29 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

DEPR:
Each integral **resistor**-capacitor assembly preferably includes an integral **resistor** 310 in series with the integral capacitor 304. Therefore, the integral **resistor** capacitor assembly provides parallel transmission **line termination** without the static power dissipation of a conventional **resistor**-only **termination**. The common conductive plate 306 is preferably grounded, such as with a via (not shown) connected to a ground pad 31 and then to an interconnect layer on the surface of the substrate (i.e. partial circuit board). Alternatively, the common conductive plate 306 could be connected to a
power supply potential. The dielectric region can be any suitable BGA package or PWB dielectric material, though the use of other dielectric materials is foreseeable. For a termination resistance of **about 50 ohms** for the integral **resistor**, a suitable capacitance is on the order of 100 pico-Farads to attain an acceptable RC time constant for the series resistor/capacitor pair. Such a capacitance can be provided within a compact area by employing suitably thin dielectric materials such as suitable high density interconnect (HDI) dielectrics or thin circuit board dielectrics conventionally employed in the fabrication of BGA interposers. Capacitance per unit area can further be enhanced by filling the polymer dielectric with a high dielectric constant ceramic powder.

US-CL-CURRENT: 326/30,326/86 ,326/93

US-PAT-NO: 6067594
DOCUMENT-IDENTIFIER: US 6067594 A
TITLE: High frequency bus system
DATE-ISSUED: May 23, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Perino; Donald V.	Los Altos	CA	N/A	N/A
Garrett, Jr.; Billy	Mountain View	CA	N/A	N/A
Wayne	Sunnyvale	CA	N/A	N/A
Liaw; Haw-Jyh	San Jose	CA	N/A	N/A
Nguyen; David	Santa Clara	CA	N/A	N/A
Nimmagadda; Srinivas	Mountain View	CA	N/A	N/A
Gasbarro; James A.	San Jose	CA	N/A	N/A
Crisp; Richard DeWitt				

US-CL-CURRENT: 710/301,326/30 ,326/86 ,326/93
ABSTRACT:
A high frequency bus system which insures uniform arrival times of high-fidelity signals to the devices on the high frequency bus, despite the use of the bus on modules and connectors. A high frequency bus system includes a first bus segment having one or more devices connected between a first and a second end. The first bus segment has at least a pair of transmission lines for propagating high frequency signals and the devices are coupled to the pair of transmission lines. The high frequency bus system also includes a second bus segment which has no devices connected to it. The second bus segment also has at least a pair of transmission lines for propagating high frequency signals. The first end of the first segment and second end of the second segment are coupled in series to form a chain of segments and when two signals are introduced to the first end of the second bus segment at the substantially the same time, they arrive at each device connected to the first bus segment at substantially the same time. Also, when two signals originate at a device connected to the first bus segment at substantially the same time, they arrive at the first end of the second bus segment at substantially the same time. Uniform arrival times hold despite the use of connectors to couple the segments together, despite the segments being located on modules, without the need for stubs, despite the presence of routing turns in the segments and despite the type of information, such as address, data or control, carried by the signals.
8 Claims, 22 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 21

BSPR:
A circuit model of a tapped line, typical of the second group of lines, is shown in FIG. 3. As shown, in this topology, each line in a group is typically connected to a module by means of a stub 360 which acts as tap off of the line as shown in FIG. 2 and FIG. 3. A stub is defined as a length of line tapped from a transmission line and having a round trip delay which is greater than the rise time (or fall time) of the signal. Since the stub 360 (160 in FIG.

2)
typically has a different impedance than the line being tapped, it is often necessary to insert a **resistor** 320, as shown in FIG. 3, in series with the stub
to mitigate the effect of reflections at the connection point of the stub to the line. If the line impedance is **about 50 ohms and the impedance of the stub**
is about 75 ohms, a **resistor** of approximately 20-25 ohms is typically chosen usually by trial and error for the best results under certain conditions. This
resistor has the possibly undesirable effect of attenuating the voltage swing of the signal as the signal passes through the **resistor,** requiring a driver on the stub to have a proportionately larger voltage swing. Another undesirable effect is the RC delay due to the added series **resistor** and the device capacitance. The **resistors** and stubs also lead to low-fidelity signals at the devices. Also, as shown in FIG. 3, the **line is terminated by resistors** 350 at both ends to minimize reflections from the ends of the **line**. This requires that the drivers on the **line** supply twice as much steady state current as compared to a **line terminated** at only one end.

US-CL-CURRENT: 174/35R,257/692 ,257/700 ,29/852

US-PAT-NO: 5499445
DOCUMENT-IDENTIFIER: US 5499445 A
TITLE: Method of making a multi-layer to package
DATE-ISSUED: March 19, 1996
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Boyle; Steven R.	Santa Clara	CA	N/A	N/A
Proebsting; Robert J.	Los Altos Hills	CA	N/A	N/A
Herndon; William H.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 29/830,174/35R ,257/692 ,257/700 ,29/852
ABSTRACT:

A multi-layered package is disclosed that employs novel shielding techniques to improve high frequency performance of the package. Shield vias are placed near conductive vias to create a two-wire transmission line with controllable characteristic impedance. Controlled transmission line impedance reduces signal reflection due to line impedance variations and ground bounce due to inductive coupling. Opposite polarity shielding technique is introduced in vertical as well as horizontal directions to reduce capacitive coupling of noise between signals and provide immunity against differential power supply noise. Signal layers disposed half way between floating shield planes provided immunity against non-common mode noise coupling. For integrated circuits with varying types of signals (e.g. CMOS and TTL and ECL type signals), the package creates electrically isolated zones to drastically reduce noise coupling between the circuits with different signal types.

6 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

BSPR:

The severity of these noise problems is magnified in an environment where low-voltage-swing signals, such as emitter coupled logic (ECL) signals, must operate in the presence of high-voltage-swing signals (e.g. CMOS signals), especially at higher frequencies. From the stand point of power consumption, it is desirable to employ low-voltage-swing signals whenever possible for any signal switching at high frequency. This is due to the fact that physical dimensions force the characteristic impedance of a transmission line to be no higher than **about 50 ohms**. To eliminate signal reflection, a 50 ohm transmission **lines is terminated** by a 50 ohm **termination resistor**. The current through the transmission line is virtually constant regardless of frequency. Therefore, power in watts defined as voltage times current (P=V.times.I) or voltage squared divided by resistance (P=V.sup.2 /R), increases directly as the square of signal voltage for a given impedance.

US-CL-CURRENT: 330/255,330/289

US-PAT-NO: 4941153
DOCUMENT-IDENTIFIER: US 4941153 A
TITLE: High-speed digital data communication system
DATE-ISSUED: July 10, 1990
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kelley; Edwin A.	Los Angeles	CA	N/A	N/A
Stone; Wade J.	Los Angeles	CA	N/A	N/A

US-CL-CURRENT: 375/257,330/255 ,330/289
ABSTRACT:

According to the invention, a high-speed digital data communication system employs current mode circuitry as input and output devices at the ends of a transmission line, such as the interconnections between integrated circuit chips. Specifically, a current mode driver switch generates output current amplitudes responsive to a source of a digital signal representative of data to be transmitted. The switch output is connected to the input of a transmission line. The output of the transmission line is connected to the input of a receiving circuit that responds to the current amplitudes and has an input at an approximately constant voltage level. The receiving circuit is a transistor connected in a common base configuration. The emitter of the transistor is connected to the output of the transmission line. The base of the transistor is connected to a constant voltage source. A pulse shaper in the form of a Schmitt trigger has positive feedback from output to input. The described current mode circuitry is incorporated into an integrated circuit chip.
7 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

DEPR:
A typical characteristic impedance of transmission line 16 in the case of a conductive path printed circuit board interconnection between chips is **about 50 to 70 ohms**. This is the same order of magnitude as the input impedance of common base transistor 54, which decreases with increasing current amplitude therethrough. To take advantage of this property of common base transistors, transistor 54 is biased so its input impedance is slightly above the characteristic impedance of transmission line 16 for the small current amplitude representing one binary value and is slightly below the characteristic impedance of transmission line 16 for the high current amplitude representing the other binary value. In this manner, the average input impedance of transistor 54 approximately matches the characteristic impedance of transmission **line** 16 without the necessity for a power dissipating **terminating resistor**.

US-CL-CURRENT: 330/286,330/296

US-PAT-NO: 4768005
DOCUMENT-IDENTIFIER: US 4768005 A
TITLE: Capacitorless DC bias lines for use with r.f. signal processing apparatus
DATE-ISSUED: August 30, 1988
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kawakami; Kenneth N.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 333/246,330/286 ,330/296
ABSTRACT:
A DC bias line module for use with an r.f. signal processing apparatus which incorporates terminating resistors, in lieu of capacitors, that are connected to the r.f. line.
7 Claims, 4 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

DEPR:
To preclude the problem experienced with capacitors in an r.f. signal processing system, r.f. coupling is provided between the DC bias lines 14 and the r.f. line 16, in accordance with this invention. As shown in FIGS. 2 and 3, the coupled r.f. **line** 16 is tied to **terminating resistors** 18a and 18b which
are preferably made of an r.f. absorbing thin film of TaN, each of which provides **about 50 ohms** of resistance. The coupled r.f. line 16 is spaced close to the DC bias line 14 so that an effective r.f. coupler region 20 (represented as a dashed line ellipse) is established.

CLPR:
6. A DC bias **line** module as in claim 1, wherein said **resistor** means comprises two **terminating resistors,** each having a resistance of **about 50 ohms**.

US-CL-CURRENT: 178/63E,375/258

US-PAT-NO: 4110711
DOCUMENT-IDENTIFIER: US 4110711 A
TITLE: Voice/data receiver coupled with a transmission line through an input transformer working into an impedance approaching a short circuit
DATE-ISSUED: August 29, 1978
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gaetano; Maur L.	Woodbridge	VA	N/A	N/A
Skrovanek; Ambroz K.	Bethesda	MD	N/A	N/A

US-CL-CURRENT: 333/32,178/63E ,375/258
ABSTRACT:

A transmission line having a fixed characteristic impedance, e.g., 600 ohms,
is coupled to a receiver through an input transformer working into a very small
impedance, e.g., 10 ohms or less. As compared to a conventional arrangement, where an input transformer works into a load nearly as high as the characteristic impedance of the line, the new arrangement has considerably better low frequency response and delay distortion characteristics. The new arrangement permits a much smaller transformer to be used if desired while retaining favorable low frequency response and delay distortion characteristics.
10 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

DEPR:
In accordance with the invention and consistent with the requirement that the transmission **line be terminated** in its characteristic impedance, the actual or virtual resistance in which the secondary winding of the input transformer is **terminated** may have values different from those indicated in the illustrative examples discussed in detail above. For example, load **resistor** R3' may be in the range of **about 10 to about 50 or 100 ohms**, it being understood that the indicated values of termination **resistors** R1' and R2' would each be reduced in resistance by an amount equivalent to half the increase in R3' over the indicated value of 10 ohms. It may also be possible to decrease the value of R3' to a new value below 10 ohms, but this may make the signal applied to amplifier 10' too low. Similarly, the virtual resistance which amplifier 10" in FIG. 3 imposes across the secondary winding of input transformer T" may have
a different value, so long as the **termination resistors** R1" and R2" are adjusted such that the **termination** impedance matches the characteristic impedance of the incoming transmission **line**. Still similarly, a different input transformer may be used in place of input transformer T' or T", with different inherent resistances of its windings, in which case the shown resistance values will have to be changed to add up to a total resistance approximately equal to the characteristic impedance of the incoming transmission line.

US-CL-CURRENT: 326/128,326/30 ,326/91

US-PAT-NO: 3560760
DOCUMENT-IDENTIFIER: US 3560760 A
TITLE: LOGIC NAND GATE CIRCUITS
DATE-ISSUED: February 2, 1971
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chung; David H.	Dallas	TX	N/A	N/A
Terrell; Bill H.	Dallas	TX	N/A	N/A

US-CL-CURRENT: 326/18,326/128 ,326/30 ,326/91
ABSTRACT:

Disclosed are logic NAND gate circuits of the type capable of driving a low impedance or a high capacitance load while maintaining relatively fast propagation speed which include a pair of output transistors of one type respectively connected to bias voltage supplies and connected in common to an output circuit, and a plurality of input transistors connected between the bases of the output transistors. A logic 1 input signal at any one of the input transistors produces a logic 0 output signal.

6 Claims, 2 Drawing figures
Number of Drawing Sheets: 1

DEPR:
In practice, it is highly desirable for the output voltage levels representative of the logic 1 and logic 0 states to be the same as the input voltage levels representative of the logic 1 and logic 0 states to permit fan-out and fan-in of the gates without intermediate circuits. Thus, assume that the logic 1 level both at the inputs and at the outputs is to be +0.4 volt, and the logic 0 level both at the inputs and at the outputs is to be -0.4
volt. In order to maintain the output 16 at a logic 1 level of the +0.4 volt, the base of output transistor 14 and hence the collectors of all of the input transistors must be at about +1.2 volts, assuming that silicon transistors are used each having a V.sub.BE of about 0.8 volt. When the output 16 is at a logic 0 level of -0.4 volt, then the base of transistor 12 and hence the collectors of the input transistors must be at about +0.4 volt. Similarly, when all of the inputs are at a logic 0 level of -0.4 volt, then the common emitters of the input transistors, and hence the base of output transistor 14, must be at about -1.2 volts, and when any one of the inputs is at a logic 1 level of +0.4 volt, the common emitters of the input transistors and the base of output transistor 14 must be at about -0.4 volt. In this case, it would be evident that the collector supply voltage V.sub.CC would have to be at least as
high as +1.2 volts, and preferably slightly higher, and that the emitter supply
voltage V.sub.EE2 would have to be at least as low as - 1.2 volts, and preferably slightly lower. The values of the resistances 30 and 32 would then be selected such that when the input voltages are all at a logic 0 level of -0.4 volt, the base of transistor 12 is at +1.2 volts, and the base of transistor 12 is at -1.2 volts, and when any one, or more, of the logic inputs is at a logic 1 level of +0.4 volt, the base of transistor 12 will be at about +0.4 volt and the base of transistor 14 will be at about -0.4 volt. In addition, care is taken to insure that the collector-base junction of the input
transistors 28 remains reverse biased and is not operated in the saturated mode. The value of **resistor** 24 is picked according to the minimum output

impedance which the circuit 10 is to drive. For example, if the transmission line 18 has a 50 ohm characteristic impedance and terminating resistor 20 is 50
ohms, it will be noted that a current of about 8 milliamperes must be passed through the load resistor 20 in order to establish the logic 1 level of +0.4 volt at output 16, and that transistor 14 must sink a current of about 8milliamperes in order to establish the logic 0 level of -0.4 volt. Thus, if the circuit 10 is to be designed to drive a minimum load of 50 ohms, then resistor 24 would be selected so as to establish a potential of about -2.0 volts at the emitter of transistor 14 when passing only the idle current of transistor 14 necessary to maintain transistor 14 operating in the nonsaturated
region, and a potential of about -1.2 volts when transistor 14 is in the higher
conductance state and is sinking the 8 milliamperes from the load 20, plus the base current from transistor 14 and any idle current from transistor 12.

	Document ID	Title	Current OR
1	US 6266730 B1	High-frequency bus system	710/300
2	US 6108212 A	Surface-mount device package having an integral passive component	361/768
3	US 6067594 A	High frequency bus system	710/301
4	US 5499445 A	Method of making a multi-layer to package	29/830
5	US 5338970 A	Multi-layered integrated circuit package with improved high frequency performance	257/659
6	US 4941153 A	High-speed digital data communication system	375/257
7	US 4768005 A	Capacitorless DC bias lines for use with r.f. signal processing apparatus	333/246
8	US 4110711 A	Voice/data receiver coupled with a transmission line through an input transformer working into an impedance approaching a short circuit	333/32
9	US 3560760 A	LOGIC NAND GATE CIRCUITS	326/18

:VALID *TDB-ACC-NO: NA8909393

DISCLOSURE TITLE: Active Terminators for CMOS Drivers

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, September 1989, US

VOLUME NUMBER: 32

ISSUE NUMBER: 4A

PAGE NUMBER: 393 - 395

PUBLICATION-DATE: September 1, 1989 (19890901)

CROSS REFERENCE: 0018-8689-32-4A-393

DISCLOSURE TEXT:

- A method is shown for substituting active transistors for **terminating** resistors on CMOS-driven transmission **lines** to provide substantial benefits in data transmission rates, power dissipation, overshoot protection, and rapid dampening of transients on the lines.

- By **terminating** data transmission **lines** in their characteristic **impedance,** rapid communications over long lines is facilitated. In instances where such lines are driven at their midpoint, characteristic **impedance terminators** at both ends of the **line** are utilized. The "quieting" of the line after data transmission is hastened because any transients reaching the extremities of the line are perfectly terminated which results in no reflected energy. These solutions proved effective for emitter coupled logic (ECL) circuit technology due to the small signal swings and superior current handling capabilities. When higher levels of integration in the CMOS technology emerged, the levels of simultaneous I/O switching increased. Also, with wider signal voltage swings, an increase in power dissipation and power transients resulted.

By terminating CMOS-driven long **lines** with an active **terminator** circuit, higher transmission rates and other transmission line performance attributes can be achieved.

- Referring to Fig. 1, a simple FET inverter circuit is shown which can be used as a transmission **line terminator**. When the transistors are matched for equal transconductance, the inverter accurately simulates a linear resistor over most of the operating range and quiescent power dissipation is greatly reduced compared with a two resistor equivalent. Termination **impedance** values of interest (30 **- 50 ohms**) can be constructed from moderate size transistors. Typically 100:1 to 200:1 W/L ratios. Fig. 2 shows the inverter circuit terminator used with four additional transistors (shown as switches) which may be activated on command. In a bus-organized system where multiple drive and receive points exist, the most advantageous position for the termination **impedance** may change from moment to moment, depending on the physical location of the drive and receive points.

Since addresses normally precede data on a bus, the direction of traffic is known in advance, allowing the system to judiciously activate and de-activate terminator circuits.

- As shown in Fig. 3, the input **impedance** of a simple CMOS

inverter wired short circuit common drain to common gate can be constructed graphically. For a given input voltage, the input current is the summation of two transistor currents each wired to ground or the power supply. In the center of the operating range where both transistors are on and in their "saturated state", the turn-off characteristics of one transistor will compensate for the turn-on characteristics of the other. If the transconductances of the two devices are chosen to be equal and the drain characteristics closely follow the theoretical formula, the square terms exactly cancel. The following applies when both transistors are in saturation:

$$IDS = \frac{K'}{2}\frac{W}{2}(VD - VT)2$$

Transconductances are set equal.

$$\frac{K'n}{2}\frac{Wn}{Ln} = \frac{K'p}{2}\frac{Wp}{Lp} = K$$

The current observed at the common drain node is: ID = K(VD2 -2VDVtn +Vtn2) - K(Vdd2 -2VddVD -2VddVtp +2VDVtp +VD2 -Vtp2) Note that the VD2 terms cancel and the only remaining constants are:

Vdd = supply voltage.

- Vtn = threshold of the n-channel transistor.
- Vtp = threshold of the p-channel transistor.
- Referring to Fig. 4, at the extremes of the operating region, only one of the two transistors is conducting and it is in the square law region. The remaining conducting transistor thus acts as a clamping diode. The active terminator can also be activated or deactivated electronically by the addition of four more transistors. Since these four transistors only charge or discharge the gate capacitance of the original two transistors, the four additional transistors can be relatively small.
- Referring to Fig. 5, typical quiescent power dissipation when the terminating **impedance** (Zo) equals 33 and active follows:

when $K = 10{,}000mA/V2$

$I(quiescent) = 11.25ma$

$Vdd = 5$ volts

$$P = 5 \times 11.25 \times 10\text{-}3 = 56.25mw$$

Typical quiescent power dissipation when the terminating **impedance** (Zo) equals 33 and passive under the same base conditions follows:

$$P = \frac{52}{132} = 189mw$$

A group of active terminators fabricated on the same semiconductor chip will track very closely. In some applications, a dummy line may be used for differential sensing as shown in Fig. 6. The dummy line may be shared with one or more other data lines.

FIG. 1

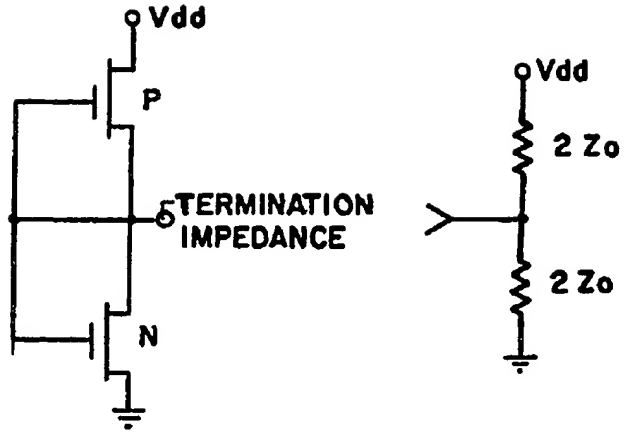


FIG. 2

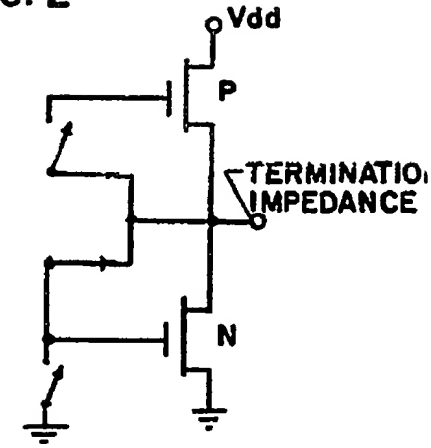


FIG. 3

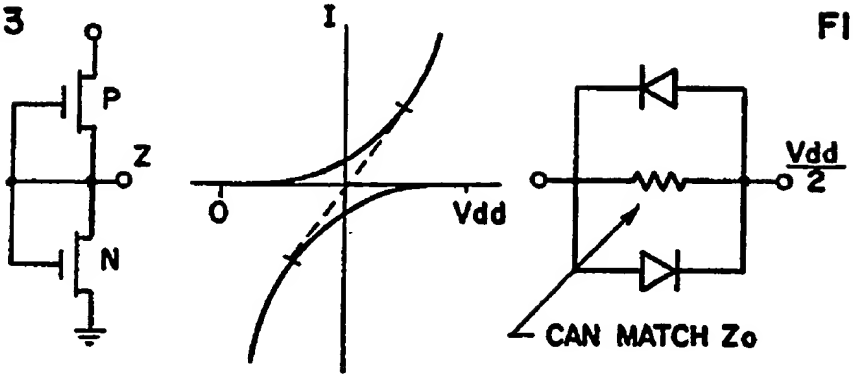


FIG. 4

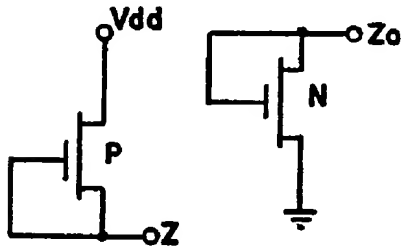


FIG. 5

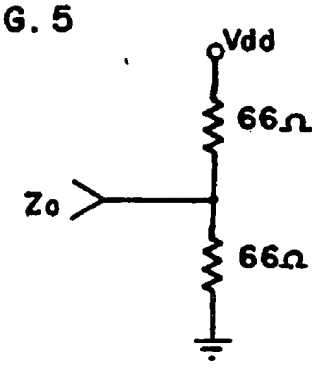
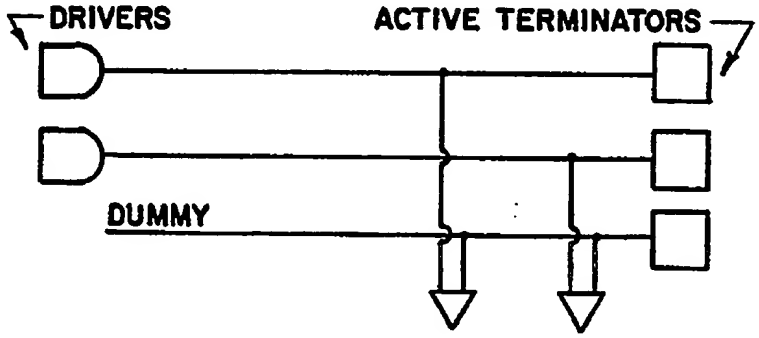


FIG. 6



DERWENT-ACC-NO: 2000-531244
DERWENT-WEEK: 200048

TITLE: Dual quadrature branch line in-phase power combiner and power splitter for communication systems, has transmission line elements to have specific characteristic impedance corresponding to transmission line

INVENTOR: BUER, K V; COOK, D L

PATENT-ASSIGNEE: MOTOROLA INC[MOTI]

PRIORITY-DATA: 1998US-0139079 (August 24, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6078227 A	June 20, 2000	N/A	007	H01P 005/16

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 6078227A	N/A	1998US-0139079	August 24, 1998

INT-CL_(IPC): H01P005/16

ABSTRACTED-PUB-NO: US 6078227A

BASIC-ABSTRACT: NOVELTY - When a high frequency signal from a transmission line
(5) enters a signal port (10), the signal is split into three signal components, which are conveyed to microstrip transmission line elements (40,50,80) via their corresponding end portions. The transmission line elements (40,50) have characteristic impedance approximately equal to characteristic impedance of the transmission line multiplied by 1.414.

DETAILED DESCRIPTION - **Terminating impedance** (60) are coupled to another end portions of upper microstrip transmission **line** elements (40,50). The **terminating** impedances are substantially equal to the value of characteristic impedances of the transmission **line** (5) which is **50 ohms**.

USE - For combining and distributing microwave signals among various components
in microwave communication systems.

ADVANTAGE - Since terminating impedance are not circuit elements, the physical or electrical length of terminating impedance is not critical thereby providing
a low cost high bandwidth dual quadrature branch line in-phase power combiner and power splitter.

DESCRIPTION OF DRAWING(S) - The figure illustrates a layout of a dual quadrature branch line in-phase power combiner and power splitter.

Transmission line 5

Signal port 10

Transmission line elements 40,50,80

Terminating impedance 60

CHOSEN-DRAWING: Dwg.1/4

TITLE-TERMS:
DUAL QUADRATURE BRANCH LINE PHASE POWER COMBINATION POWER SPLIT COMMUNICATE SYSTEM TRANSMISSION LINE ELEMENT SPECIFIC CHARACTERISTIC IMPEDANCE CORRESPOND TRANSMISSION LINE

DERWENT-CLASS: W02

EPI-CODES: W02-A02B1; W02-A02D;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2000-392773

DERWENT-ACC-NO: 1987-235460
DERWENT-WEEK: 198733

TITLE: Stable high speed semiconductor device - eliminates branches in connection for perfect impedance matched transmission

INVENTOR: EMORI, S; WATANABE, Y ; EMORL, S

PATENT-ASSIGNEE: FUJITSU LTD[FUIT], WATANABE YD[WATAI]

PRIORITY-DATA: 1986JP-0024181 (February 7, 1986) , 1987JP-0000079 (February 6, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 8704855 A	August 13, 1987	J	040	N/A
DE 3787137 G	September 30, 1993	N/A	000	H01L 021/60
EP 258444 A	March 9, 1988	E	000	N/A
EP 258444 A4	June 14, 1989	N/A	000	N/A
EP 258444 B1	August 25, 1993	E	021	H01L 021/60
JP 62501120 X	January 7, 1988	N/A	000	N/A
US 4920406 A	April 24, 1990	N/A	000	N/A

DESIGNATED-STATES: JP KR US DE FR GB DE FR GB DE FR GB

CITED-DOCUMENTS: JP57104235; JP61152047 ; No-Citns. ; 01Jnl.Ref

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
WO 8704855A	N/A	1987WO-JP00079	February 6, 1987
DE 3787137G	N/A	1987DE-3787137	February 6, 1987
DE 3787137G	N/A	1987EP-0901126	February 6, 1987
DE 3787137G	N/A	1987WO-JP00079	February 6, 1987
DE 3787137G	Based on	EP 258444	N/A
DE 3787137G	Based on	WO 8704855	N/A
EP 258444A	N/A	1987EP-0901126	February 6, 1987
EP 258444A4	N/A	1987EP-0901126	N/A
EP 258444B1	N/A	1987EP-0901126	February 6, 1987
EP 258444B1	N/A	1987WO-JP00079	February 6, 1987
EP 258444B1	Based on	WO 8704855	N/A
JP62501120X	N/A	1987JP-0000079	February 6, 1987
US 4920406A	N/A	1987US-0124944	October 7, 1987

INT-CL_(IPC): H01C023/02; H01L021/60 ; H04L025/02

ABSTRACTED-PUB-NO: EP 258444B
BASIC-ABSTRACT: A semiconductor device has an IC circuit (1) which drives two IC circuits (2, 3) via a micro strip **line** (4) printed on a board (10) and is **terminated with an impedance** matching resistor of **50 ohms** (45). Each receive-side IC (2;3) has a pair of package leads (211, 212; 311,312), of which
the outer ends are connected to a transmission line of the drive side (211;311)
and to the terminal side (212;312), whilst the inner ends are connected to pads
(251,252; 351,352) on a chip (23;33) with bonding wires (241,241; 341,342).

Thus a transmission line is formed from the drive-side IC (1) to the terminating resistor (45) without any branch and with perfect impedance matching.

ADVANTAGE - Stable operation ensured in high-speed IC's.

ABSTRACTED-PUB-NO: US 4920406A
EQUIVALENT-ABSTRACTS: A semiconductor device comprising a driving-side integrated circuit (1) which is electrically connected to at least two receiving-side integrated circuits (2, 3) by means of a transmission line (4) interconnec ting each receiving-side integrated circuit (2, 3) of the device, said driving-side integrated circuit (1) when in use transmitting a driving signal to each of said receiving-side integrated circuits (2, 3) via said transmission line (4), characterised in that the said integrated circuits (1, 2, 3) are connected together in series via pad means (251, 252; 351, 352) provided on each receiving-side integrated circuit (2, 3) of the device, each of said pad means (251, 252; 351, 252) being connected, via a pair of package leads (211, 212, 311, 312) of the circuit (2, 3) concerned, between consecutive
sections of said transmission line (4) such that said driving signal is transmitted via the pad means (251, 252; 351, 352) of each receiving-si de integrated circuit (2, 3).

The semiconductor devices operatively connectable to a drive side transmission line and a to a terminating side transmission line, comprising: the semiconductor device has a pair of package leads each with an external end and and internal end. The external end of the package lead is electrically connectable to the drive side transmission line. The external end of another package lead is electrically connectable to the terminating side transmission line. An integrated circuit has pads and the internal ends electrically connected to integrated circuit through at least one of the pads.

A pair of conductors have two ends. The first ends are respectively connected to the pair of package leads and the second ends are connected to at least one of the pads. The internal ends are electrically connected together via the pair of conductors and at least one of the pads.

USE/ADVANTAGE - For drive and terminating side of transmission line. Eliminates high-speed signal disturbance. Improved operation. (18pp)

WO 8704855A

CHOSEN-DRAWING: Dwg.1/21 Dwg.6/21

TITLE-TERMS:

STABILISED HIGH SPEED SEMICONDUCTOR DEVICE ELIMINATE BRANCH CONNECT PERFECT IMPEDANCE MATCH TRANSMISSION

DERWENT-CLASS: U11 U21 W01

EPI-CODES: U11-D01A; U11-D03A6; U11-D03B1; U11-D03C1; U21-C03D; W01-A08X;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1987-176171

US-CL-CURRENT: 307/106,327/126 ,327/170 ,333/156 ,333/245 ,365/198

US-PAT-NO: 3656009
DOCUMENT-IDENTIFIER: US 3656009 A
TITLE: NON-LINEAR TRANSMISSION LINE CURRENT DRIVER
DATE-ISSUED: April 11, 1972
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chen; Chung-Ho	Plymouth Meeting	PA	N/A	N/A

US-CL-CURRENT: 327/108,307/106 ,327/126 ,327/170 ,333/156 ,333/245 ,365/198
ABSTRACT:
There is disclosed herein an arrangement for developing a fast rise time current pulse in a transmission line. The pulse is produced in the line in steps until the final value of current is reached. By developing the drive current in incremental steps undesirable overshoot is eliminated.
10 Claims, 2 Drawing figures
Number of Drawing Sheets: 1

BSPR:
Another shortcoming of using an ordinary transmission **line termination** resistor
equal to the characteristic **impedance** for the drive **line** of a wire memory is that the Z.sub.o would have a conservative value of **50 ohms**. At a required drive voltage and current of 50 volts and 1 ampere, respectively, and for a 50 **percent** duty factor, the power dissipation would be 25 watts. This may be lowered somewhat by various expedients but this figure is relatively close for later comparison purposes. In any event, it can be readily appreciated that if
every word **line** in a plated wire memory were so **terminated**, not only would there be a large space utilization due to the size of such a resistor but furthermore there would be great heat dissipation.

US-CL-CURRENT: 333/17.2,361/111 ,361/113 ,361/58 ,455/283 ,455/287 ,455/305

US-PAT-NO: 4930035
DOCUMENT-IDENTIFIER: US 4930035 A
TITLE: Radio frequency limiter circuit
DATE-ISSUED: May 29, 1990
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Viana; Luis M.	Melrose	MA	N/A	N/A
Cuozzo; Robert A.	North Andover	MA	N/A	N/A
Miceli; Michael L.	Hingham	MA	N/A	N/A
Whitney; Kent A.	Lunenburg	MA	N/A	N/A

US-CL-CURRENT: 361/54,333/17.2 ,361/111 ,361/113 ,361/58 ,455/283 ,455/287 ,455/305

ABSTRACT:
A radio frequency limiter having a radio frequency power divider having an input and a plurality of outputs; at least one diode connected in shunt with each one of the outputs of the power divider; and, a power combiner having an output and a plurality of inputs, each one of such inputs being connected to a corresponding one of the outputs of the power divider. With such arrangement, the insertion loss of such limiter is reduced compared to a limiter having a like number of diodes connected in shunt at a common point of a single transmission line. Therefore, the reduced insertion loss means that the impedance matching circuit required will not limit the maximum operating frequency to the degree an impedance matching circuit of similar complexity will limit the maximum operating frequency required for a limiter having the same number of diodes but using a single transmission line.
5 Claims, 4 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

DEPR:
Referring now to FIG. 1B, a limiter 10' according to the prior art is shown to include a single transmission line section 14' coupled to input port 16'. A pair of p-i-n diodes 20'a, 20'b are shown **terminating** input transmission **line** section 14' at junction 19'. An output transmission line section 28' connects junction 19' to output port 26'. The p-i-n diodes 20'a, 20'b are here assumed to be identical to diodes 20a, 20b described in connection with FIG. 1A. Further, the characteristic **impedance** of transmission line section 14' is Z.sub.o, here again **50 ohms**. The insertion loss per diode 20'a, 20'b is here again 0.3 db as it was for each of diodes 20a, 20b of FIG. 1A. Further, under high power conditions the resistance of each one of the forward biased diodes 20'a, 20'b is R, here 60 ohms as it was for diodes 20a, 20b. Thus, considering
first the insertion loss of limiter 10' at the low power level condition, if the power applied to input port 16' is again Pi, each diode 20'a, 20'b, will provide 0.3 db of insertion loss. Therefore, each one of the diodes 20'a, 20'b
will transmit 93 **percent** of the power fed to junction 19' with the result that 7 **percent** of the power is lost per diode, for a total of 14% and thus only 86 **percent** of the power applied to input port 16' will appear at output port 26' under low power conditions. The insertion loss of the power limiter 10' is thus 0.6 db. Hence, the limiter 10 shown in FIG. 1A has 0.3 db less insertion loss compared with limiter 10' shown in FIG. 1B; however, it is noted that the above analysis assumed that the power divider 12 used in the limiter 10, and not used in the limiter 10', does in the practical case, have a finite

insertion loss. However, the insertion loss of the power divider/combiner 12, 22 through proper design may be constructed to be less than 0.3 db, and more typically may be 0.1 db. Thus, in the practical case, the insertion loss of limiter 10 (FIG. 1A) according to the invention is about 0.4 db while the insertion loss of limiter 10' (FIG. 1B) according to the prior art is 0.6 db. This reduced insertion means that any input **impedance** matching circuit required
will not limit the maximum operating frequency of the limiter 10 to the degree required for the input **impedance** matching circuit required for the prior art limiter 10'.

PGPUB-DOCUMENT-NUMBER: 20010035768
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010035768 A1

TITLE: Output driver circuit with well-controlled output impedance

PUBLICATION-DATE: November 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Garlepp, Bruno Werner	Mountain View	CA	US	
Donnelly, Kevin S.	San Francisco	CA	US	
Zerbe, Jared LeVan	Palo Alto	CA	US	

US-CL-CURRENT: 326/30

ABSTRACT:

An output driver circuit for driving a signal onto a signal line. The output driver circuit comprises at least one driver circuit and a passive network. The passive network is configured to limit the variation in the output impedance of the output driver circuit. The output driver circuit thus provides an output impedance that closely matches the loaded impedance of the signal line at all times so as to minimize secondary reflections on the signal line.

ASNM:
Rambus Inc.

BSTX:
[0003] For example, FIG. 1 illustrates a prior art digital system 1 including a plurality of devices 2, a signal transmitting device 3 and a signal line 4. The transmitting device 3 contains an output driver circuit 5 that generates a single-ended signal for output onto the signal line 4. The devices 2 are connected to the signal line 4 at various points to receive the signal. The signal **line** 4 includes a conductor 12, a **termination** resistor R.sub.T and a **termination** voltage V.sub.Term. The termination resistor R.sub.T is connected to the end of the conductor 12 opposite the end connected to the output driver circuit 5. The termination resistor R.sub.T absorbs the incident signal, thereby preventing reflections of the signal from occurring at the end of the conductor 12. The termination resistor R.sub.T is also connected to the termination voltage V.sub.Term. The termination voltage V.sub.Term is used to raise the voltage of the conductor 12 to the high voltage level V.sub.oh.

BSTX:
[0008] A third cause for the clock jitter are the primary and secondary reflections of the clock signal produced on the clock line 8. Primary reflections are reflections of the clock signal produced along the conductor 10 by taps along the conductor at which the DRAMs 11 are connected and by the termination resistor R.sub.T. The reflections travel back towards the clock driver circuit 9. These reflections occur because of an impedance mismatch or discontinuity in the clock **line** 8 caused by the taps and/or the **termination** resistor. The primary reflections in turn cause secondary reflections to

occur
at the output of the clock driver circuit 9. The secondary reflections occur because the output impedance of the clock driver circuit 9, which acts as a high output impedance current source, is significantly greater than the loaded impedance Z.sub.0 of the clock line 8. The secondary reflections travel back down the conductor 10, thereby disturbing the clock signal waveform and causing
jitter in the clock signal received by the DRAMs 11.

DETX:
[0058] The differential clock **lines** 17 also include two **termination** resistors R.sub.T1 and R.sub.T2. A first end of each termination resistor R.sub.T1 and R.sub.T2 is connected to the end of the respective conductor 18 or 19 opposite the end connected to the clock driver 15. A second end of the termination resistor R.sub.T1 is connected to a second end of the termination resistor R.sub.T2 at a node Ch_mid to form an electrical connection between conductors 18 and 19. Assuming the signals CTM and CTMN are truly differential, i.e., the
signals are 180 degrees out-of-phase with each other, the node Ch_mid will appear as a differential ground with the conductors 18 and 19 being terminated with the termination resistors R.sub.T1 and R.sub.T2, respectively. The termination resistors R.sub.T1 and R.sub.T2 prevent reflections of the differential signals CTM and CTMN from occurring at the end of the conductors 18 and 19, respectively. In order to minimize the signal reflections, the resistance of the **termination** resistors R.sub.T1 and R.sub.T2 is set to equal the loaded impedance Z.sub.0 of the differential clock **lines** 17. Optionally, a
capacitor C.sub.End is connected between the node Ch_mid and a power supply (as
shown by the dotted lines in FIG. 9) to reinforce the differential ground.

US-CL-CURRENT: 365/194

US-PAT-NO: 6324120
DOCUMENT-IDENTIFIER: US 6324120 B1
TITLE: Memory device having a variable data output length
DATE-ISSUED: November 27, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Farmwald; Michael	Berkeley	CA	N/A	N/A
Horowitz; Mark	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 365/233,365/194
ABSTRACT:

A synchronous memory device and methods of operation and controlling such a device. The method of controlling the memory device includes providing block size information to the memory device, synchronously with respect to an external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a read request. The method further includes issuing a first read request to the memory device, wherein the memory device receives the first read request synchronously with respect to a transition of the external clock signal.
39 Claims, 18 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 15

ASNM:
Rambus Inc.

BSPR:
High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The **bus lines** are controlled-impedance, doubly-**terminated lines**. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5-2 nH. Each
device 15, 16, 17, shown in FIG. 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

DEPR:
By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The **bus** of a preferred embodiment of the present invention consists of a set of resistor-**terminated** controlled impedance transmission **lines** which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus. These
devices add lumped capacitance to the lines which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the
bus impedance is likely to be on the order of 25 ohms and the propagation velocity about c/4 (c=the speed of light) or 7.5 cm/ns. To operate at a 2 ns

data rate, the transit time on the bus should preferably be kept under 1 ns, to
leave 1 ns for the setup and hold time of the input receivers (described below)
plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm
for maximum performance. Lower performance systems may have much longer lines,
e.g. a 4 ns bus may have 24 cm lines (3 ns transit time, 1 ns setup and hold time).

US-CL-CURRENT: 326/30

US-PAT-NO: 6321282
DOCUMENT-IDENTIFIER: US 6321282 B1
TITLE: Apparatus and method for topography dependent signaling
DATE-ISSUED: November 20, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Horowitz; Mark A.	Menlo Park	CA	N/A	N/A
Barth; Richard M.	Palo Alto	CA	N/A	N/A
Hampel; Craig E.	San Jose	CA	N/A	N/A
Moncayo; Alfredo	Redwood City	CA	N/A	N/A
Donnelly; Kevin S.	Los Altos	CA	N/A	N/A
Zerbe; Jared L.	Woodside	CA	N/A	N/A

US-CL-CURRENT: 710/104,326/30
ABSTRACT:

Bus communications are optimized by adjusting signal characteristics in accordance with one or more topography dependent parameters. In a bus transmitter, a transmit signal characteristic is adjusted in accordance with a topography dependent parameter. A port in the bus transmitter receives the topography dependent parameter for later use by the parameter adjustment circuitry. The parameter adjustment circuitry adjusts a parameter control signal in accordance with the topography dependent parameter, which is coupled to the output driver. Prior to driving an output signal onto a bus, the output
driver adjusts the transmit signal characteristic in accordance with the parameter control signal. In a bus receiver, a receive signal characteristic is adjusted in response to a topography dependent parameter. A port associated
with the bus receiver receives the topography dependent parameter and stores it
in a register. Parameter adjustment circuitry adjusts a control signal in accordance with the stored topography dependent parameter. An input buffer receives an input signal from a bus coupling the receiver to a transmitter of the input signal. The input buffer generates a first signal from the input signal by adjusting a the parameter of the input signal in accordance with the control signal.
50 Claims, 32 Drawing figures
Exemplary Claim Number: 26
Number of Drawing Sheets: 22

ASNM:
Rambus Inc.

BSPR:
A bus system is a chip-to-chip electronic communications system in which one or
more slave devices are connected to, and communicate with, a master device through shared bus signal lines. FIG. 1 illustrates in block diagram form a bus system. The bus system includes a Master control device (M) that communicates with one or more Slave devices (D) via a bi-directional data bus. Typically, the bidirectional data bus comprises a plurality of bus signal lines, but for simplicity, FIG. 1 illustrates only one bus signal line. The terms bus signal line and channel are used synonymously herein. Thus, it will be understood that the data bus includes many channels, one for each bit of data. Each **bus** signal **line terminates** on one side at an I/O pin of the master

device and **terminates** on its other side at one end of a resistive **terminator** (T). The resistance of the **terminator** is closely matched to the loaded impedance, Z.sub.L, of the **bus** signal **line** to minimize reflections and absorb signals sent down the **bus** signal **line** toward the **terminator**. The opposite end of the **terminator** is connected to a voltage supply that provides an AC ground and sets the DC **termination** voltage of the **bus** signal **line**. The positions along the **bus** signal **line** tapped by the Master **terminator,** and Slaves are labeled P.sub.M, P.sub.T, and P.sub.1 -P.sub.N, respectively.

BSPR:
Bus systems are typically designed to work with several configurations to allow
system flexibility. For example, the bus may have several connector slots for inserting individual Slaves or Modules of Slaves, and each Module may have different numbers of devices. This allows the user to change the number of chips that operate in the bus system, allowing small, medium, and large systems
to be configured without complex engineering changes, such as changes to the printed circuit board layout. FIG. 2 illustrates a Bus System that provides this flexibility by providing three connectors for three Slave Modules. This figure does not necessarily illustrate the physical layout of an actual system,
but shows the electrical connections of the Bus System. The first Module is shown with eight Slaves, the second with four Slaves, and the third Modules with no Slaves. The third Module serves only to electrically connect the **terminator to the bus** signal **line**. For simplicity, this configuration can be referred to as an 8-4-0 configuration, and many other configurations are possible by inserting different Modules into the three connector slots (e.g. 8-8-8, 4-0-0, etc.). As in FIG. 1, FIG. 2 designates the points at which each device taps the bus signal line (e.g. Slave B.sub.2 taps the bus signal line at
point P.sub.B2). The Bus System of FIG. 2 is very flexible; however, this flexibility results in configuration-dependent and position-dependent channel characteristics that lead to signaling complexities and reduce the reliability of data transmission through the system.

US-CL-CURRENT: 365/194

US-PAT-NO: 6314051
DOCUMENT-IDENTIFIER: US 6314051 B1
TITLE: Memory device having write latency
DATE-ISSUED: November 6, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Farmwald; Michael	Berkeley	CA	N/A	N/A
Horowitz; Mark	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 365/233,365/194
ABSTRACT:

A memory device having a plurality of memory cells, the memory device comprising clock receiver circuitry to receive an external clock signal, and input receiver circuitry to sample, in response to a write request, a first portion of data after a number of clock cycles of the external clock signal transpire. The first portion of data is sampled synchronously with respect to the external clock signal.

43 Claims, 18 Drawing figures
Exemplary Claim Number: 34
Number of Drawing Sheets: 15

ASNM:
Rambus Inc.

BSPR:
High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The **bus lines** are controlled-impedance, doubly-**terminated lines**. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5-2 nH. Each
device 15, 16, 17, shown in FIG. 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

DEPR:
By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The **bus** of a preferred embodiment of the present invention consists of a set of resistor-**terminated** controlled impedance transmission **lines** which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus. These
devices add lumped capacitance to the lines which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the
bus impedance is likely to be on the order of 25 ohms and the propagation velocity about c/4 (c=the speed of light) or 7.5 cm/ns. To operate at a 2 ns data rate, the transit time on the bus should preferably be kept under 1 ns, to

leave 1 ns for the setup and hold time of the input receivers (described below)
plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm
for maximum performance. Lower performance systems may have much longer lines,
e.g. a 4 ns bus may have 24 cm lines (3 ns transit time, 1 ns setup and hold time).

US-CL-CURRENT: 326/30

US-PAT-NO: 6308232
DOCUMENT-IDENTIFIER: US 6308232 B1
TITLE: Electronically moveable terminator and method for using same in a memory system
DATE-ISSUED: October 23, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gasbarro; James Anthony	Mountain View	CA	N/A	N/A

US-CL-CURRENT: 710/100,326/30
ABSTRACT:
An expandable memory system having a plurality of memory devices, each with an electronically activated terminator is disclosed. Also a method for detecting the last memory device arranged along a data **bus** connecting a memory controller with the memory devices, and activating its active **terminator** is disclosed.
17 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

ASNM:
Rambus Inc.

ABPL:
An expandable memory system having a plurality of memory devices, each with an electronically activated terminator is disclosed. Also a method for detecting the last memory device arranged along a data **bus** connecting a memory controller
with the memory devices, and activating its active **terminator** is disclosed.

BSPR:
The bi-directional data bus comprises a number of signal lines, but for simplicity, only one signal line is shown in the drawings. Each signal **line** **terminates** at one end at an Input/Output (I/O) pin of the memory controller and
terminates at the other end at a resistive **terminator** (T). The resistance of **terminator** (T) is closely matched to the loaded impedance of the signal **line** in
order to minimize reflections on the signal **line** and absorb signals sent down the signal **line** towards the **terminator**. The other end of the **terminator** (T) is
connected to a voltage supply (V.sub.T) which provides an AC ground and sets the DC **termination** voltage on the signal **line**.

BSPR:
Because the signal **line** is nominally pulled to the value of the **termination** voltage, this voltage can serve as one of the logical states for digital signals transmitted on the signal **line**. Switched current sources, such as open
drain NMOS devices, can then be used as the signal driver circuits in either the master or memory devices. These simple signal drivers produce the logical data signals by either shutting off or sinking current as required to produce the logical states ("1" and "0"). For example, the termination voltage (V.sub.HI) can serve as the high voltage state and low logical state "0", and

a
low voltage state (V.sub.LO) can serve as the high logical state "1" where V.sub.LO =(V.sub.T -I.sub.O Z.sub.L) and I.sub.O is the nominal current sunk by
a current source driver when it is turned "ON."

BSPR:
When the memory controller transmits signals to one or more of the memory devices, it "sees" the full impedance, Z.sub.L, of the signal line and produces
full swing signals of magnitude V.sub.SWING =(V.sub.HI -V.sub.LO) that travel down the signal line. As long as the I/O pins to the memory devices form short
stubs **terminated** in a high impedance, little energy is lost and minimal parasitic reflections are produced as the signals propagate down the signal **line** and pass by the memory devices. As a rule of thumb, the stubs can be considered short if their electrical lengths are shorter than the rise and/or fall times of the signals. The signals transmitted by the memory controller propagate down the signal **line,** pass by all the memory devices, where they can be sensed, and eventually **terminate at the terminator**.

BSPR:
The situation is somewhat different when a memory device transmits to the memory controller. Each driver circuit in the memory device effectively "sees"
two signal **lines**; one traveling towards the memory controller, and the other traveling towards the **terminator**. Thus, the net impedance seen by each driver circuit is 1/2 Z.sub.L. Assuming the driver circuits in the memory devices also sink I.sub.O current, the signals that emerge from the memory device I/O pins split at the signal **line** with half the signal voltage traveling towards the memory controller and half the signal voltage traveling towards the **terminator**. The half-V.sub.SWING signals that travel towards the terminator pass by any intervening memory devices and then simply terminate at the matched
impedance of the terminator. However, the half-V.sub.SWING signals that travel
towards the memory controller pass by any intervening memory devices and then encounter open circuits when they reach the memory controller I/O pins. This effectively open circuit condition causes the signals from the memory device to
double in voltage at the memory controller I/O pins as the signal energy is reflected back down the signal **line** towards the **terminator**. Thus, although only half the normal signal voltage is sent by the memory devices towards the memory controller, the memory controller still receives a full voltage swing signal at its I/O pins due to the signal reflection. This is true provided the
signal **line terminates** in a high impedance (i.e., an open circuit) at the memory controller. The other memory devices in the system will see half-normal
amplitude signals pass by their I/O pins at least twice per memory device transmission. However, since the memory system is designed to transmit data from a memory device to the memory controller, and not between memory devices, this signal line condition is acceptable. Accordingly, no matter which device in the memory system is transmitting data, a full swing signal appears at the input of the intended receiving device.

BSPR:
As can be appreciated from the foregoing, memory system impedance is a critical

system design and performance parameter. Absent a careful balance between the various memory system components noted above, the signal line impedance will depart from its desired impedance. A signal **line** impedance mismatch will result in unwanted signal reflections from the **terminator,** and in increased signal **line** noise associated with such undesired reflections. Increased signal
line noise may, at some point, preclude discrimination of data signals at the memory devices or memory controller. This need to match signal line impedance has, to date, precluded the implementation of a truly expandable high speed memory system. That is, because the signal **line** impedance will necessarily change with additional loading caused by the connection of additional memory devices or memory modules to the data **bus,** memory system expansion required a high level of technical support and significant hardware level intervention, such as swapping out the existing **terminator** with a new **terminator** having an impedance consistent with the additional loading.

BSPR:
Alternatively, a physically moveable terminator can be placed between the populated portion of the data bas which has a first impedance and the unpopulated portion of the data which is terminated in a predetermined impedance and has a second impedance different from the first. This physically
moveable **terminator,** or impedance balancing connector, is inserted in the first
unoccupied "slot" on the data **bus** in order to maintain proper data **bus** impedance under variable loading conditions. U.S. Pat. No 4,595,923 more fully explains this approach.

BSPR:
Both of these conventional approaches to maintaining signal line impedance following the connection of additional devices require direct technician intervention. That is, a trained technician employing a special, additional part (i.e., a new **terminator** or an impedance balancing connector) is required to maintain signal **line** impedance and compensate for the additional signal **line**
loading.

BSPR:
The present invention provides a readily expandable, high-speed memory system. Expansion is contemplated for memory systems incorporating a plurality of memory devices, memory modules, or slots along a data bus. By use of an active
terminator, a memory controller may balance data **bus** impedance when one or more
additional memory devices, memory modules are added to a memory system.

BSPR:
In one aspect, the present invention provides a memory system comprising; a memory controller connected to a plurality of memory devices (or memory modules) via a data **bus,** the data **bus** comprising a first portion having a first
impedance, and a second portion having a second impedance, wherein at least one
of the plurality of memory devices (or memory modules) comprises an active **terminator** having a third impedance, such that upon activation of the active **terminator,** the third impedance is placed in parallel with the second impedance
to balance the first and second impedances.

BSPR:
In another aspect, the present invention provides a memory system comprising; a
memory controller connected to a data **bus**, the data **bus** comprising a plurality of slots, each slot adapted to receive a memory module and comprising an active
terminator responsive to a control signal from the memory controller.

BSPR:
In yet another aspect, the present invention provides a method of balancing impedance between first and second portions of a data **bus** in a memory system, the memory system comprising a memory controller and a plurality of memory devices connected via a serial initialization **line** and a channel including the data **bus**, the method comprising; determining in the memory controller one memory device located last on the data **bus**, and activating an active **terminator**
in the one memory device to balance the first and second portions of the data **bus**.

DRPR:
FIG. 5 is a schematic diagram illustrating another aspect of the present invention in which an active **terminator** is associated with a data **bus** slot;

DEPR:
A high speed memory system is disclosed which incorporates an electronically moveable terminator. The electronically moveable **terminator** is a switchable component preferably associated with a memory device, a memory module, or a slot associated with memory system data **bus**. The term "data bus" as used throughout denotes one or more signal lines by which data is communicated between a memory controller and one or more memory devices or memory modules. It is recognized that the actual data bus may be part of a larger channel which
includes additional signal lines carrying address and control information, or which comprises a multiplexed set of signal lines carrying data information, control information, and address information.

DEPR:
Conceptually, the present invention provides a system and method by which a number of memory devices, memory modules, or data bus slots are implemented with the foregoing switchable component. The switchable component may take many forms and several examples are given below. Regardless of its actual form
or the nature of the device into which it is incorporated, the switchable component will be referred to as an "active **terminator**." Any one of the memory devices, memory modules, or data **bus** slots incorporating the active **terminator** may be switched or "activated" by the memory controller to provide the data **bus**
impedance necessary for proper memory system operation.

DEPR:
Typically, each memory device or memory module will incorporate an active **terminator** so that "standard" parts may be manufactured and placed, without data **bus** impedance related distinctions, anywhere along the data **bus**. Once the
data **bus** has been populated with an appropriate number of memory devices or memory modules, the last one of these devices will have its active **terminator** activated, i.e, switched ON. This system and method will be discussed in

additional detailed below with reference to several exemplary embodiments. These embodiments are drawn from presently preferred memory system configurations. They have been simplified in many ways to focus the following discussion on the present invention and not on other well understood aspects of
memory system design. The examples must be given in some context in order to be useful. However, the present invention is not limited to the teaching context or the specific exemplary embodiments presented. Memory system design is by its very nature is a flexible and evolving endeavor. Thus, many variations to the simple examples given below are contemplated within the scope
of the present invention as it is defined by the claims below.

DEPR:
FIG. 3 is a block diagram of a memory system according to the present invention
in which a memory controller 10 is connected to a plurality of memory devices 20 (including D.sub.1, D.sub.2, . . . D.sub.N), each memory device incorporating an active terminator 21. The memory devices are connected by and
positioned along a data **bus** 12 which **terminates into a terminator** 14 connected to a terminal voltage V.sub.T. Impedance along data **bus** 12 may be viewed as having two components; a first component Z.sub.1 between the memory controller and the "last" memory device D.sub.N, and a second component Z.sub.2 between D.sub.N and the data **bus terminator**.

DEPR:
The impedance Z.sub.1 is typically different from impedance Z.sub.2. Ideally, Z.sub.1 and Z.sub.2 should have the same impedance to avoid undesired signal reflections on the data bus, and unbalanced signal propagation by memory devices onto the data bus. The presence of an active **terminator** in memory device D.sub.N provides the memory system with an ability to equalize these impedances and balance the respective portions of the data **bus**. In effect, Z.sub.1 =Z.sub.AT.parallel.Z.sub.2, where Z.sub.AT is the internal impedance of
the active terminator in memory device D.sub.N when it is switched ON. In one presently preferred example, the combined loaded impedance for Z.sub.1 is about
25 ohms. The impedance of Z.sub.2 is typically 50 ohms. Accordingly, the impedance of Z.sub.AT is defined to be 50 ohms.

DEPR:
Thus, once the data **bus** is populated with a desired number of memory devices, the active **terminator** of the last memory device is activated to equalize Z.sub.1 and Z.sub.2. Data bus impedance is not dependent on a static, predefined number of memory devices arranged along the data bus. Further, when
one or more additional memory devices are added to the data **bus**, there is no requirement to alter data **bus terminator** (T) or rearrange a physically moveable
terminator on the data **bus**. Rather, upon system initialization following the connection of additional memory devices, the memory controller will recognize the new "last" memory device D.sub.N, and turn ON the corresponding active terminator. This electronic "moving" of the terminator is preferably done as part of the conventional memory system initialization routine which recognizes and identifies the resources in the memory system.

DEPR:
Alternatively, the active **terminator** may be associated with each slot along

the
data **bus** as illustrated in FIG. 5. Here, rather than relying on the memory device or module (which may be manufactured by a number of different vendors) to provide the active **terminator,** the memory system incorporate an active **terminator** 41 into each data **bus** slot 40. The last slot filled (or populated) by a memory module will receive a signal from the memory controller during memory system initialization to turn ON the active terminator.

DEPR:
Whether the active **terminator** is switched in the last memory device, the last memory module, or the last populated slot, memory devices on the data **bus** "see"
balanced impedances as between sections of the data **bus** running towards the memory controller and the data **bus terminator**. Accordingly, the 1/2 V.sub.SWING signaling scheme explained above works well. Further, the matched impedances preclude undesired signal reflections on the data bus, thereby eliminating a potentially significant noise source.

CLPR:
10. A method of balancing impedance between first and second portions of a data **bus** in a memory system, the memory system comprising a memory controller and a plurality of memory devices connected via a serial initialization **line** and a channel including the data **bus,** wherein the data **bus** connects the memory controller at a first end and a resistive **terminator** at a second end, the method comprising:

CLPV:
a memory controller connected to a plurality of memory devices via a data **bus,** wherein the data **bus terminates** in the memory controller at a first end and at a resistive **terminator** at a second end;

CLPV:
a resistive **terminator** connected to a second end of the data **bus;**

CLPV:
wherein the data **bus** comprises a plurality of slots arranged between the first and second ends of the data **bus,** each slot being adapted to receive a memory module and comprising an active **terminator** responsive to a control signal from the memory controller.

CLPV:
determining in the memory controller one memory device located last on the data
bus closest to the resistive **terminator;** and,

CLPV:
activating an active **terminator** in the one memory device to balance the first and second portions of the data **bus**.

CLPV:
a memory controller connected to a first end of a data **bus,** and a resistive **terminator** connected to second end of the data **bus,** wherein the data **bus** comprises a first portion having a first impedance, and a second portion having
a second impedance,

CLPV:

a plurality of memory devices arranged along the data **bus** between the first and
second ends from a first memory device closest to the memory controller to a last memory device closest to the resistive **terminator,**

US-CL-CURRENT: 365/233

US-PAT-NO: 6304937
DOCUMENT-IDENTIFIER: US 6304937 B1
TITLE: Method of operation of a memory controller
DATE-ISSUED: October 16, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Farmwald; Michael	Berkeley	CA	N/A	N/A
Horowitz; Mark	Palo Alto	CA	N/A	N/A

ABSTRACT:
A method of operation of a memory controller device, the method of operation comprises issuing a write request to a memory device synchronously with respect to an external clock signal, wherein in response to the write request, a memory device inputs first and second portions of data. The method of operation further includes outputting the first portion of data synchronously with respect to a first edge transition of an external clock signal; and outputting the second portion of data from the bus synchronously with respect to a second edge transition of the external clock signal. The first and second edge transitions of the external clock signal are of transitions of the same clock cycle.
40 Claims, 17 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 14

ASNM:
Rambus Inc.

BSPR:
High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The **bus lines** are controlled-impedance, doubly-**terminated lines**. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5-2 nH. Each device 15, 16, 17, shown in FIG. 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

DEPR:
By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The **bus** of a preferred embodiment of the present invention consists of a set of resistor-**terminated** controlled impedance transmission **lines** which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus. These devices add lumped capacitance to the lines which both lowers the impedance of

the lines and decreases the transmission speed. In the loaded environment, the
bus impedance is likely to be on the order of 25 ohms and the propagation
velocity about c/4 (c=the speed of light) or 7.5 cm/ns. To operate at a 2 ns
data rate, the transit time on the bus should preferably be kept under 1 ns, to
leave 1 ns for the setup and hold time of the input receivers (described below)
plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm
for maximum performance. Lower performance systems may have much longer lines,
e.g. a 4 ns bus may have 24 cm lines (3 ns transit time, 1 ns setup and hold
time).

US-CL-CURRENT: 327/530

US-PAT-NO: 6294934
DOCUMENT-IDENTIFIER: US 6294934 B1
TITLE: Current control technique
DATE-ISSUED: September 25, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Garrett, Jr.; Billy	Mountain View	CA	N/A	N/A
Wayne	late of Palo Alto	CA	N/A	N/A
Dillon; John B.	Sunnyvale	CA	N/A	N/A
Ching; Michael Tak-Kei	San Jose	CA	N/A	N/A
Stonecypher; William F.	San Jose	CA	N/A	N/A
Chan; Andy Peng-Pui	Mountain View	CA	N/A	N/A
Griffin; Matthew M.				

US-CL-CURRENT: 327/108,327/530
ABSTRACT:
An output driver circuit and current control technique to facilitate high-speed buses with low noise is used to interface with high-speed dynamic RAMs (DRAMs). The architecture includes the following components: an input isolation block (120), an analog voltage divider (104), an input comparator (125), a sampling latch (130), a current control counter (115), and a bitwise output driver (output driver A 107 and output driver B 111).
31 Claims, 12 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

ASNM:
Rambus Inc.

BSPR:
The master employs an adjustable current sink as a driver for each bus line that it drives. The current sink turns on to drive the voltage on the **bus line**, V.sub.out, to a voltage closer to ground and turns off to allow a **termination** resistor, R.sub.term, on the **bus line** to pull the **bus line** closer to the **terminator** voltage, V.sub.term. The current in the driver, I.sub.d, is set by a digital counter whose count is determined from a feedback circuit having a comparator. If the count is all zeros then no current flows in the driver and the voltage on the **bus line**, V.sub.out, is the **termination** voltage, V.sub.term. If the count is all ones, then the maximum current flows in the driver and the voltage on the bus line, V.sub.out, equals V.sub.term -I.sub.d *R.sub.term.

US-PAT-NO: 6273759
DOCUMENT-IDENTIFIER: US 6273759 B1
TITLE: Multi-slot connector with integrated bus providing contact between adjacent modules
DATE-ISSUED: August 14, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Perino; Donald V.	Los Altos	CA	N/A	N/A
Gamini; Nader	San Jose	CA	N/A	N/A

US-CL-CURRENT: 439/631
ABSTRACT:

The present invention provides an electrical connector having an integrated bus to provide a signal path having a properly matched impedance. The electrical connector includes a housing formed with a number of slots adapted to receive a module. Electrical contacts are placed between adjacent slots in the electrical connector, such that the combination of electrical contacts and inserted modules forms the integrated bus. Since inter-slot connections are not made through the motherboard, the noted impedance discontinuities do not arise. The electrical contacts generally include electrical signal contacts and ground contacts generally formed within the housing of the electrical connector but include metal contacts which extend into adjacent slots to form a portion of the integrated bus. The plurality of modules thus connected may include a termination module, and/or a dummy module. The **bus** may be **terminated in a termination** resistor found on the motherboard, the electrical connector, or a **termination** module inserted into the electrical connector. Alternatively, one or more of the modules may incorporate an integrated circuit having an electronically actuated termination resistor.

15 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 13

ASNM:
Rambus INC

ABPL:
The present invention provides an electrical connector having an integrated bus to provide a signal path having a properly matched impedance. The electrical connector includes a housing formed with a number of slots adapted to receive a module. Electrical contacts are placed between adjacent slots in the electrical connector, such that the combination of electrical contacts and inserted modules forms the integrated bus. Since inter-slot connections are not made through the motherboard, the noted impedance discontinuities do not arise. The electrical contacts generally include electrical signal contacts and ground contacts generally formed within the housing of the electrical connector but include metal contacts which extend into adjacent slots to form a portion of the integrated bus. The plurality of modules thus connected may include a termination module, and/or a dummy module. The **bus** may be **terminated in a termination** resistor found on the motherboard, the electrical connector, or a **termination** module inserted into the electrical connector. Alternatively,

one or more of the modules may incorporate an integrated circuit having an electronically actuated termination resistor.

BSPR:
In many contemporary **bus** systems, a **bus** runs between a controller 12 and a **bus termination** impedance 15. The bus typically comprises multiple signal lines communicating data and/or control information between the controller and one or more of the integrated circuits on one or more of modules 13. Controller 12 may take many forms including a microprocessor or a memory controller. The bus may range in size from a single signal line to a collection of complex signal line structures. The one or more integrated circuit(s) 14 on each module may be memory device(s) or logic device(s).

BSPR:
The increasing demand for data bandwidth from contemporary bus systems drives the development of impedance controlled buses within such systems. That is, increasing bus system clock speeds require carefully controlled signal line impedances in order to effectively communicate data and control information. At contemporary clock speeds, which already range above several hundred MHz, impedance mismatches on the bus will create unwanted signal reflections which act as noise signals on the bus. Recognizing the need to balance signal **line** impedances, conventional **bus** systems **terminate the bus** in a characteristic impedance 15.

BSPR:
Data and control signals traversing the **bus** from controller 12 to **termination** impedance 15 travel the signal path 16 shown in FIG. 1A. Of note, some portions of the signal path pass through the several connectors 11 and other portions of the path pass through the motherboard 10. The transmission performance of such a "mixed" signal path has generally been acceptable in bus systems running a relatively lower frequencies. However, the transmission performance of this type of signal path has proved increasingly inadequate as bus system operating at higher frequencies.

BSPR:
In theory, the composition of the motherboard and the connectors mounted on the motherboard, as well as the signal **line** traces forming the **bus,** should produce a consistent impedance matched to **termination** impedance 15. Actual practice is, however, far from theory. The motherboard is often manufactured by a different entity than the one manufacturing connectors 11 or modules 13. In fact, the printed circuit boards (PCBs) commonly used as motherboards are notoriously variable in their final composition and implementation, and therefore their effective impedance. Further, motherboard impedances tend to vary from unit to unit depending on actual finished trace width, dielectric thickness and composition. As a result, signal path 16 shown in FIG. 1A often suffers from multiple impedance discontinuities caused by the signal path transitions from motherboard-to-connector, and from connector-to-motherboard.

BSPR:
The **bus** may be **terminated in a termination** resistor found on the motherboard, the electrical connector, or a **termination** module inserted into the electrical connector. Alternatively, one or more of the modules may incorporate an integrated circuit having an electronically actuated termination resistor.

DRPR:
FIGS. 9A, 9B, and 9C illustrate exemplary **termination** options for **bus** systems

configured in accordance with the present invention.

DEPR:
The terms "first" and "last" are used to describe connector slots in relation to one another. A first connector slot is typically the closest slot to the controller and the farthest slot from the termination resistor. However, this designation assumes a contemporary **bus** system description in which command signals originate in a controller, traverse the length of the **bus**, and end at the **termination** resistor. With this assumption, the first slot is typically first populated with a module in order to provide a "base" (i.e., a minimal system) having the shortest signal propagation time. Thereafter, slots in the electrical connector are normally populated with modules in order from first to
last.

DEPR:
The embodiment shown in FIG. 6 provides a shorter overall bus length in relation to the number of modules actually used in the system. For example, when first installed the **bus** system shown in FIG. 6 included only first module 61 inserted in slot 60a and **termination** module 64 inserted in slot 60b. Subsequently, modules 62 and 63 were added to the bus system. As each new module is added to the system, the termination module 64 is moved to the next unoccupied slot in the electrical connector. This approach allows for the variable configuration of the **bus** system, but does so at the price of an electrical connector slot which must be used to connect **termination** module 64.

DEPR:
Several possibilities for connecting the termination resistor are summarized in
the illustrations of FIGS. 9A, 9b and 9C. In the **bus** system contemplated in FIG. 9A, the electrical connector comprises a fixed **termination** resistor connected after the last slot. (See, e.g, the connector shown in FIG. 5). This type of electrical connector increases the number of slots made available for module connections when compared to the connector shown in FIG. 6. However, the electrical connector of FIG. 9A requires the use of one or more connection (or dummy) modules 91 for slots not having a module, since **bus** continuity must be provided from the first slot of the electrical connector to the **termination** resistor, regardless of the number of modules actually populating the connector.

DEPR:
The electrical connector shown in FIG. 9B is a hybrid of the connector shown in
FIG. 5 and the bus system implementation contemplated in FIG. 6. Here, a fixed
termination resistor is provided after the last slot, but a **termination** module 92 may be used to "shorten" the **bus** length where fewer than the maximum number of modules are inserted in the electrical connector.

CLPR:
4. The **bus** system of claim 3, wherein the last module comprises a **termination** module.

CLPR:
9. The **bus** system of claim 8, wherein the motherboard further comprises a **termination** resistor, and the **bus** system further comprises:

CLPR:

10. The **bus** system of claim 8, wherein the plurality of modules comprises a **termination** module.

CLPR:
12. The **bus** system of claim 11, wherein the motherboard further comprises a **termination** resistor, and the **bus** system further comprises:

CLPR:
13. The **bus** system of claim 11, wherein the plurality of modules comprises a **termination** module.

CLPR:
14. The **bus** system of claim 3, wherein the plurality of modules comprises a module having an integrated **termination** resistor.

CLPR:
15. The **bus** system of claim 3, wherein the plurality of modules comprises a module having an electrically actuated **termination** resistor.

CLPV:
wherein the plurality of electrical contacts further comprises a first electrical contact connected to a high speed **bus** on the motherboard and having a metal contact surface extending through a wall of the first slot, and a last electrical contact connected to a **termination** resistor on the motherboard and having a metal contact surface extending through a wall of the Nth slot.

US-CL-CURRENT: 326/27,326/30

US-PAT-NO: 6198307
DOCUMENT-IDENTIFIER: US 6198307 B1
TITLE: Output driver circuit with well-controlled output impedance
DATE-ISSUED: March 6, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Garlepp; Bruno Werner	Mountain View	CA	N/A	N/A
Donnelly; Kevin S.	San Francisco	CA	N/A	N/A
Zerbe; Jared LeVan	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 326/83,326/27 ,326/30
ABSTRACT:

An output driver circuit for driving a signal onto a signal line. The output driver circuit comprises at least one driver circuit and a passive network. The passive network is configured to limit the variation in the output impedance of the output driver circuit. The output driver circuit thus provides an output impedance that closely matches the loaded impedance of the signal line at all times so as to minimize secondary reflections on the signal line.

14 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 20

ASNM:
Rambus Inc.

BSPR:
For example, FIG. 1 illustrates a prior art digital system 1 including a plurality of devices 2, a signal transmitting device 3 and a signal line 4. The transmitting device 3 contains an output driver circuit 5 that generates a single-ended signal for output onto the signal line 4. The devices 2 are connected to the signal line 4 at various points to receive the signal. The signal **line** 4 includes a conductor 12, a **termination** resistor R.sub.T and a **termination** voltage V.sub.Term. The termination resistor R.sub.T is connected to the end of the conductor 12 opposite the end connected to the output driver circuit 5. The termination resistor R.sub.T absorbs the incident signal, thereby preventing reflections of the signal from occurring at the end of the conductor 12. The termination resistor R.sub.T is also connected to the termination voltage V.sub.Term. The termination voltage V.sub.Term is used to raise the voltage of the conductor 12 to the high voltage level V.sub.oh.

BSPR:
A third cause for the clock jitter are the primary and secondary reflections of
the clock signal produced on the clock line 8. Primary reflections are reflections of the clock signal produced along the conductor 10 by taps along the conductor at which the DRAMs 11 are connected and by the termination resistor R.sub.T. The reflections travel back towards the clock driver circuit
9. These reflections occur because of an impedance mismatch or discontinuity in the clock **line** 8 caused by the taps and/or the **termination** resistor. The primary reflections in turn cause secondary reflections to occur at the output of the clock driver circuit 9. The secondary reflections occur because the output impedance of the clock driver circuit 9, which acts as a high output impedance current source, is significantly greater than the loaded impedance

Z.sub.0 of the clock line 8. The secondary reflections travel back down the conductor 10, thereby disturbing the clock signal waveform and causing jitter in the clock signal received by the DFIAMs 11.

DEPR:
The differential clock **lines** 17 also include two **termination** resistors R.sub.T1
and R.sub.T2. A first end of each termination resistor R.sub.T1 and R.sub.T2 is connected to the end of the respective conductor 18 or 19 opposite the end connected to the clock driver 15. A second end of the termination resistor R.sub.T1 is connected to a second end of the termination resistor R.sub.T2 at a
node Ch_mid to form an electrical connection between conductors 18 and 19. Assuming the signals CTM and CTMN are truly differential, i.e., the signals are
180 degrees out-of-phase with each other, the node Ch_mid will appear as a differential ground with the conductors 18 and 19 being terminated with the termination resistors R.sub.T1 and R.sub.T2, respectively. The termination resistors R.sub.T1 and R.sub.T2 prevent reflections of the differential signals
CTM and CTMN from occurring at the end of the conductors 18 and 19, respectively. In order to minimize the signal reflections, the resistance of the **termination** resistors R.sub.T1 and R.sub.T2 is set to equal the loaded impedance Z.sub.0 of the differential clock **lines** 17. Optionally, a capacitor C.sub.End is connected between the node Ch_mid and a power supply (as shown by the dotted lines in FIG. 9) to reinforce the differential ground.

US-CL-CURRENT: 365/194

US-PAT-NO: 6101152
DOCUMENT-IDENTIFIER: US 6101152 A
TITLE: Method of operating a synchronous memory device
DATE-ISSUED: August 8, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Farmwald; Michael	Berkeley	CA	N/A	N/A
Horowitz; Mark	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 365/233,365/194
ABSTRACT:

A synchronous memory device having a plurality of memory cells and a method of operation thereof. The memory device comprising: receiver circuitry to receive a first external clock signal; and output driver circuitry, to output data after a preprogrammed number of clock cycles of the first external clock signal transpire. The data is output synchronously with respect to the first external clock signal. The method of operation comprises: receiving a request for a read operation; sensing data in a portion of the plurality of sense amplifiers in response to the request for a read operation; and outputting the data after a preprogrammed delay time transpires. The method may further include receiving an external clock signal wherein the preprogrammed time delay
is representative of a fixed number of clock cycles of the external clock signal. The data is output synchronously with respect to the first external clock signal.
25 Claims, 18 Drawing figures
Exemplary Claim Number: 11
Number of Drawing Sheets: 15

ASNM:
Rambus Inc.

BSPR:
High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The **bus lines** are controlled-impedance, doubly-**terminated lines**. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5-2 nH. Each
device 15, 16, 17, shown in FIG. 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

DEPR:
By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The **bus** of a preferred embodiment of the present invention consists of a set of resistor-**terminated** controlled impedance transmission **lines** which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus.

These
devices add lumped capacitance to the lines which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the
bus impedance in likely to be on the order of 25 ohms and the propagation velocity about c/4 (c=the speed of light) or 7.5 cm/ns. To operate at a 2 ns data rate, the transit time on the bus should preferably be kept under 1 ns, to
leave 1 ns for the setup and hold time of the input receivers (described below)
plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm
for maximum performance. Lower performance systems may have much longer lines,
e.g. a 4 ns bus may have 24 cm lines (3 ns transit time, 1 ns setup and hold time).

US-CL-CURRENT: 327/530

US-PAT-NO: 6094075
DOCUMENT-IDENTIFIER: US 6094075 A
TITLE: Current control technique
DATE-ISSUED: July 25, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Garrett, Jr.; Billy	Mountain View	CA	N/A	N/A
Wayne	late of Palo Alto	CA	N/A	N/A
Dillon, deceased; John	Sunnyvale	CA	N/A	N/A
B.	San Jose	CA	N/A	N/A
Ching; Michael Tak-Kei	San Jose	CA	N/A	N/A
Stonecypher; William F.	Mountain View	CA	N/A	N/A
Chan; Andy Peng-Pui				
Griffin; Matthew M.				

US-CL-CURRENT: 327/108,327/530
ABSTRACT:
An output driver circuit and current control technique to facilitate high-speed buses with low noise is used to interface with high-speed dynamic RAMs (DRAMs). The architecture includes the following components: an input isolation block (120), an analog voltage divider (104), an input comparator (125), a sampling latch (130), a current control counter (115), and a bitwise output driver (output driver A 107 and output driver B 111).
33 Claims, 12 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

ASNM:
Rambus Incorporated

BSPR:
The master employs an adjustable current sink as a driver for each bus line that it drives. The current sink turns on to drive the voltage on the **bus line**, V.sub.out, to a voltage closer to ground and turns off to allow a **termination** resistor, R.sub.term, on the **bus line** to pull the **bus line** closer to the **terminator** voltage, V.sub.term. The current in the driver, I.sub.d, is set by a digital counter whose count is determined from a feedback circuit having a comparator. If the count is all zeros then no current flows in the driver and the voltage on the **bus line**, V.sub.out, is the **termination** voltage, V.sub.term. If the count is all ones, then the maximum current flows in the driver and the voltage on the bus line, V.sub.out, equals V.sub.term -I.sub.d *R.sub.term.

US-CL-CURRENT: 365/189.02,365/230.02 ,365/233 ,710/3 ,710/36 ,710/51 ,710/61 ,710/9

US-PAT-NO: 6070222
DOCUMENT-IDENTIFIER: US 6070222 A
TITLE: Synchronous memory device having identification register
DATE-ISSUED: May 30, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Farmwald; Michael	Berkeley	CA	N/A	N/A
Horowitz; Mark	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 711/105,365/189.02 ,365/230.02 ,365/233 ,710/3 ,710/36 ,710/51 ,710/61 ,710/9

ABSTRACT:
The present invention is directed to a synchronous memory device having a memory cell array divided into a plurality of subarrays, including first and second subarrays each having a plurality of subarray sections. The memory device further includes a device identification register to store an identification code to identify the memory device. A first subarray section in the memory device includes a first internal I/O line to access data from a first memory cell location in the first subarray section and a second internal I/O line to access data from a second memory cell location in the first subarray section. A second subarray section in the memory device includes a first internal I/O line to access data from a third memory cell location in the second subarray section and a second internal I/O line to access data from a fourth memory cell location in the second subarray section. In addition, the memory device includes output driver circuitry, including a first output driver and a second output driver, to output data onto the external bus in response to the read request when the identification information corresponds to the identification code. Multiplexer circuitry couples the first internal I/O line of the first subarray section to an input of the first output driver and couples the first internal I/O line of the second subarray section to an input of the second output driver in response to a clock edge of a first internal clock signal; and couples the second internal I/O line of the first subarray section to an input of the first output driver and couples the second internal I/O line of the second subarray section to an input of the second output driver in response to the clock edge of the second internal clock signal.

37 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 17

ASNM:
Rambus Inc.

BSPR:
High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The **bus lines** are controlled-impedance, doubly-**terminated lines**. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm).

In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5-2 nH. Each
device 15, 16, 17, shown in FIG. 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

DEPR:
By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The **bus** of a preferred embodiment of the present invention consists of a set of resistor**-terminated** controlled impedance transmission **lines** which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus. These
devices add lumped capacitance to the lines which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the
bus impedance is likely to be on the order of 25 ohms and the propagation velocity about c/4 (c=the speed of light) or 7.5 cm/ns. To operate at a 2 ns data rate, the transit time on the bus should preferably be kept under 1 ns, to
leave 1 ns for the setup and hold time of the input receivers (described below)
plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm
for maximum performance. Lower performance systems may have much longer lines,
e.g. a 4 ns bus may have 24 cm lines (3 ns transit time, 1 ns setup and hold time).

CLPR:
37. The memory system of claim 28 wherein the **bus** further includes a plurality
of low voltage swing conductors **terminated** by an impedance to a power source.

US-CL-CURRENT: 326/30,326/86 ,710/107

US-PAT-NO: 6009487
DOCUMENT-IDENTIFIER: US 6009487 A
TITLE: Method and apparatus for setting a current of an output driver for the high speed bus
DATE-ISSUED: December 28, 1999
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Davis; Paul Gregory	San Jose	CA	N/A	N/A
Batra; Pradeep	Santa Clara	CA	N/A	N/A
Dillon; John B.	Palo Alto	CA	N/A	N/A
Krishnamohan;	San Jose	CA	N/A	N/A
Karnamadakala	Mountain View	CA	N/A	N/A
Gasbarro; James A.				

US-CL-CURRENT: 710/105,326/30 ,326/86 ,710/107
ABSTRACT:
In a system comprising a current controlling device and a plurality of signal lines coupled to the current controlling device, wherein the current controlling device has an output driver including a register, an improved method for setting a current of the output driver for at least one of the plurality of signal lines. The improved method determines a reference register-setting for the register of the current controlling device. The reference register-setting corresponds to a reference voltage for at least one of the plurality of signal lines. A target register-setting is then determined
for the register based on the reference register-setting. The target register-setting corresponds to a target voltage for at least one of the plurality of signal lines, wherein the target voltage produces an appropriate swing about the reference voltage. An operational register-setting is then determined for the register based on the target register-setting. The current of the output driver for at least one of the plurality of signal lines is then set based on the operational register-setting so that a swing about the reference voltage is optimal.
55 Claims, 12 Drawing figures
Exemplary Claim Number: 37
Number of Drawing Sheets: 12

ASNM:
Rambus Inc.

BSPR:
Additionally variations between comparison circuits in the master, variations in the reference and circuit voltages in the master and the slave, and variations in **bus termination** may also cause errors in the register setting process disclosed in Horowitz.

DEPR:
BusData [8:0] comprise nine matched transmission **lines** each having controlled impedance and **terminated** on one end by a **termination** resistor R. The nine **termination** resistors are collectively referred to as **termination** resistors 20.
Termination resistors 20 are coupled to Vterm. BusCtrl **line** 14 is **terminated by termination** resistor 23 coupled to Vterm. BusEnable **line** 15 is **terminated by termination** resistor 21 coupled to Vterm. CLkFromMaster **line** 16b and ClkToMaster **line** 16a are coupled to clock 35 and **terminated by termination**

resistor 22 coupled to Vterm.

DEPR:
In FIG. 2, current mode driver 100 is coupled to data transmission line 111 via
output pad 110. Data transmission line 111 is one of the data transmission lines of bus 30 which is in turn coupled to master 11. Master 11 is coupled to
current calibrator 40. Transmission **line** 111 is coupled to the **termination** voltage Vterm via **termination** resistor 112 which is one of resistors 20 illustrated in FIG. 1.

DEPR:
SWINGMULTIPLIER may be predetermined with knowledge of the non-ideal current source characteristics of output transistor array 101. FIG. 12 illustrates a plurality of transistor curves for transistor array 101, where I is the current
of transistor array 101 and V is the voltage generated on bus 30. Load **line** 1202 is the operating load **line** for transistor array 101 and may be expressed as I=((Vterm-V)/Rterm), where Rterm is one of the **terminating** resistors 20 illustrated in FIG. 1. Load line 1202 has a maximum current Iterm, and a maximum voltage Vterm (VOH). Transistor curve 1204 corresponds to the condition where a particular number of transistors in transistor array 101 are turned on in order to approximately generate Vref and Iall on bus 30 at operating point 1208. Transistor curve 1206 corresponds to the condition where
another particular number of transistors in transistor array 101 are turned on in order to approximately generate the operational voltage VOL (VOLop) and IOLop on bus 30 at operating point 1210.

DEPR:
The transmission **lines of bus** 30 are sampled a number of times to mitigate variations between output drivers in slave 212, variations in the comparison circuits in master 11, variations in the reference and circuit voltages in master 11 and slave 212, and variations in **bus termination** of each of the transmission **lines of bus** 30.

DEPR:
The methods illustrated in FIGS. 4 through 11 may also be used to set an operating current of a current source in either a slave or master device for a **bus** architecture that includes a modular **bus** with single or double **termination**.
The modular **bus** includes a **terminated** motherboard data net for communicating data signals between a master and one or more motherboard slaves. A socket is used for coupling the data signals between the motherboard data net and a terminated module data net of a removable module. The module data net communicates the data signals between the master and one or more module devices
affixed to the removable module. The module device may comprise slave devices.
The data signal swing and level of reflection of the data signals are substantially independent of the presence of the module. The modular **bus** has a
known fixed impedance when the removable module is not coupled to the **terminated** motherboard data net. When the removable module is coupled to the **terminated** motherboard data net the impedance of the modular **bus** is altered in a known amount.

US-CL-CURRENT: 365/238.5

US-PAT-NO: 5841715
DOCUMENT-IDENTIFIER: US 5841715 A
TITLE: Integrated circuit I/O using high performance bus interface
DATE-ISSUED: November 24, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Farmwald; Michael	Berkeley	CA	N/A	N/A
Horowitz; Mark	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 365/203,365/238.5
ABSTRACT:

The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected to a bus, where the bus includes a plurality of bus lines for carrying substantially
all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

The present invention also includes a protocol for master and slave devices to communicate on the bus and for registers in each device to differentiate each device and allow bus requests to be directed to a single or to all devices. The present invention includes modifications to prior-art devices to allow them to implement the new features of this invention. In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide.
11 Claims, 17 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 14

ASNM:
Rambus, Inc.

BSPR:
High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The **bus lines** are controlled-impedance, doubly-**terminated lines**. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5-2 nH. Each
device 15, 16, 17, shown in FIG. 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

DEPR:
By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The **bus** of a preferred embodiment of the present invention consists of a set of resistor-**terminated** controlled impedance

transmission **lines** which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus. These devices add lumped capacitance to the lines which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the bus impedance is likely to be on the order of 25 ohms and the propagation velocity about c/4 (c=the speed of light) or 7.5 cm/ns. To operate at a 2 ns data rate, the transit time on the bus should preferably be kept under 1 ns, to leave 1 ns for the setup and hold time of the input receivers (described below) plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm for maximum performance. Lower performance systems may have much longer lines, e.g. a 4 ns bus may have 24 cm lines (3 ns transit time, 1 ns setup and hold time).

US-CL-CURRENT: 327/292

US-PAT-NO: 5663661
DOCUMENT-IDENTIFIER: US 5663661 A
TITLE: Modular **bus** with single or double parallel **termination**
DATE-ISSUED: September 2, 1997
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dillon; John B.	Palo Alto	CA	N/A	N/A
Nimmagadda; Srinivas	Santa Clara	CA	N/A	N/A
Moncayo; Alfredo	Redwood City	CA	N/A	N/A

US-CL-CURRENT: 326/30,327/292
ABSTRACT:

A modular **bus** permitting single or double **termination** is described. The **bus** includes a **terminated** motherboard data net for communicating data signals between a master and one or more motherboard devices. A socket is used for coupling the data signals between the motherboard data net and a terminated module data net of a removable module. The module data net communicates the data signals between the master and one or more module devices. The data signal swing and level of reflection of the data signals are substantially independent of the presence of the module.

32 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

TTL:
Modular **bus** with single or double parallel **termination**

ASNM:
Rambus, Inc.

ABPL:
A modular **bus** permitting single or double **termination** is described. The **bus** includes a **terminated** motherboard data net for communicating data signals between a master and one or more motherboard devices. A socket is used for coupling the data signals between the motherboard data net and a terminated module data net of a removable module. The module data net communicates the data signals between the master and one or more module devices. The data signal swing and level of reflection of the data signals are substantially independent of the presence of the module.

BSPR:
This invention relates to the field of bus architectures. In particular this invention relates to a high speed modular **bus** architecture that converts between single **termination** without a module and double **termination** with a module.

BSPR:
One prior art method of decreasing the effect of reflections requires the use of terminators. A **terminator** is a dissipative load, typically a resistor, located at the end of a transmission **line**. The **terminator** is chosen to have an impedance that matches the characteristic impedance of the transmission **line**. Prior art termination architectures include series termination and parallel

termination.

BSPR:
In series **termination, the terminating** resistor is placed in series with the device driving the transmission **line**. In parallel **termination,** the device drives the transmission **line** directly and a **terminator** is placed at one or both ends of the transmission **line**. A **bus** with a parallel **termination** at one end of the **bus** is referred to as a single parallel **termination bus**. Alternatively such a **bus** may be called a singly **terminated bus**. A **bus** with parallel **terminations** at both ends is referred to as a double parallel **termination bus**. Alternatively such a **bus** may be called a doubly **terminated bus**.

BSPR:
In one prior art singly **terminated bus, the terminator** is replaced with an extended **bus** segment containing a **terminator**. The extended bus segment includes the expansion modules. In another prior art singly **terminated bus,** all expansion sockets on the **bus** are populated with either a functional module or a "dummy module". The functional module is a module such as a memory expansion module. The dummy module in this case is a module designed to provide the same effective load as a functional module. Thus in either of these cases the **bus** is always maintained as a singly **terminated bus** either with or without the modules.

BSPR:
Double parallel **termination** is commonly used in high speed **bus** architectures. In one prior art doubly **terminated bus** architecture, modules are plugged into or removed from a doubly **terminated bus**. The modules effectively tap into the bus. Bus discontinuities will result whenever a tap does not have a module plugged into it. In some cases the modules are inserted or removed regardless of the impedance mismatch. One disadvantage of this technique is the degradation of system performance as described above. Alternatively, the taps can be populated with dummy modules. One disadvantage of this technique is the complication and cost of additional dummy modules. Thus the **bus** is effectively maintained as a double parallel **termination bus**. One disadvantage of such a system is that dummy modules must be available to replace the removed modules.

BSPR:
In one prior art doubly **terminated bus,** the modules include **bus** segments that are daisy-chained together as more modules are added to the system. The modules are connected onto a **bus** already having a **terminator**. The last module would have to be a dummy module having a second terminator. This architecture always requires a dummy terminator module as the last module in the chain. In addition to the disadvantage of requiring the dummy module, this architecture requires "shuffling" the dummy module to another location every time the number of modules on the bus changes.

BSPR:
In view of limitations of known systems and methods, one of the objectives of the present invention is to provide a modular **bus** that permits either single or double parallel **termination**. The **bus** includes a **terminated** motherboard data net for communicating data signals between a master and one or more

motherboard
devices. A socket is used for coupling the data signals between the motherboard data net and a terminated module data net of a removable module. The module data net communicates the data signals between the master and one or
more module devices. The data signal swing and level of reflection of the data
signals are substantially independent of the presence of the module.

BSPR:
A bus having a clock signal swing substantially independent of the presence of the module is also described. The **bus** includes a **terminated** motherboard clock net for communicating a first clock signal to one or more motherboard devices. A clock signal splitter provides the first clock signal and a second clock signal from a source clock signal. A socket communicates at least one of the first clock signal and the second clock signal to a terminated module clock net
for one or more module devices.

DEPR:
FIG. 1 illustrates the clock and data net topologies for a single channel bus on a motherboard with module 120 plugged in. "Bus" refers collectively to the bus segments coupled to master ASIC 110. In other words, "bus" refers to the motherboard bus and the module bus collectively when the module is plugged in. Without the module "bus" refers only to the motherboard bus. The bus includes module bus 102 and motherboard bus 104. The motherboard **bus** is a singly **terminated bus**. The module **bus is also terminated**. Without the module, the **bus** is a singly **terminated bus**. With the module, the **bus** is a doubly **terminated bus**. The module bus includes module clock net 166 and module data net 172. The motherboard bus 104 includes motherboard clock net 165 and motherboard data net 174.

DEPR:
FIG. 2 illustrates data net 170 modeled as a transmission line. Referring also
to FIG. 1, the portion of the motherboard data net from master ASIC 110 to the socket for inserting the module is modeled as stub 210. A stub is a section of
transmission **line** connected to the main transmission **line** and containing an essentially non-dissipative **termination**. The motherboard data net includes segment 240 attributable to the motherboard slaves and segment 250 from the last motherboard slave to the motherboard data net terminating resistor (192). The module data net includes segment 220 attributable to the module slaves and segment 230 from the last module slave to the module data net terminating resistor (182). Socket 260 couples the module data net to motherboard data net
including stub 210. Terminating resistors 182 and 192 are not shown in this data net model.

CLPR:
6. The **bus** of claim 1 wherein the motherboard net comprises a motherboard data
net, wherein the module net comprises a module data net, wherein the motherboard data net and the module data net are coupled to form a doubly **terminated** data net when the module is present.

CLPR:
7. The **bus** of claim 1 wherein the motherboard net comprises a motherboard clock net for communicating a first clock signal, wherein the module net

comprises a module clock net, wherein the motherboard clock net and the module clock net are coupled to form a doubly **terminated** clock net when the module is present.

CLPR:
9. The **bus** of claim 8 wherein the second clock signal is communicated to a non-**terminated** end of the module clock net, wherein the socket couples a module
clock net transmit node to a motherboard clock net transmit node, wherein the socket couples a module clock net receive node to a motherboard clock net receive node.

CLPR:
12. The **bus** of claim 8 wherein the second clock signal is communicated to a non-**terminated** end of the module clock net, wherein the first clock signal is not communicated to the module clock net.

CLPR:
13. The **bus** of claim 8 wherein a **terminating** resistance of the module clock net and the motherboard clock net is in a range of 45 to 55 ohms.

CLPR:
23. The **bus** of claim 18 wherein a **terminating** resistance of each of the module
clock net, the module data net, the motherboard clock net, and the motherboard data net is in a range of 45 to 55 ohms.

CLPV:
(A) setting a register setting of the master to a first value, wherein the **bus** couples the master to the slave, wherein the **bus** is doubly **terminated** when the removable module is coupled to the **bus, wherein the bus** is singly **terminated** when the removable module is not coupled to the **bus**;

US-CL-CURRENT: 327/147,331/2 ,365/230.02 ,365/230.08 ,713/401

US-PAT-NO: 5657481
DOCUMENT-IDENTIFIER: US 5657481 A
TITLE: Memory device with a phase locked loop circuitry
DATE-ISSUED: August 12, 1997
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Farmwald; Michael	Berkeley	CA	N/A	N/A
Horowitz; Mark	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 713/400,327/147 ,331/2 ,365/230.02 ,365/230.08 ,713/401
ABSTRACT:

A clock signal generation apparatus for a memory device of a data processing system is described for generating an internal clock signal for the memory device that is synchronized with an external clock signal. The data processing system includes a transmission line for transmitting a global clock signal to the memory device. A first receiving circuit is coupled to a first point of the transmission line for receiving the global clock signal at the first point and for generating a first local clock signal. A first delay circuitry delays the first local clock signal to be a first delayed clock signal such that the first delayed local clock signal is synchronized with the global clock signal received at the first point of the transmission line. The first delay circuitry provides a first variable delay to the first delayed local clock signal. A second receiving circuit is coupled to the second point of the transmission line for receiving the global clock signal at the second point and for generating a second local clock signal. A second delay circuitry delays the second local clock signal to be a second delayed clock signal such that the second delayed local clock signal is synchronized with the global clock signal received at the second point of the transmission line. The second delay circuitry provides a second variable delay to the second delayed local clock signal. A third delay circuitry is coupled to receive the first and second local clock signals for generating the internal clock signal for the memory device at a timing that is halfway between the first and second local clock signals.

18 Claims, 17 Drawing figures
Exemplary Claim Number: 8
Number of Drawing Sheets: 11

ASNM:
Rambus, Inc.

BSPR:
High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The **bus lines** are controlled-impedance, doubly-**terminated lines**. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5-2 nH. Each

device 15, 16, 17, shown in FIG. 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

DEPR:
By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The **bus** of a preferred embodiment of the present invention consists of a set of resistor-**terminated** controlled impedance transmission **lines** which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus. These devices add lumped capacitance to the lines which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the bus impedance is likely to be on the order of 25 ohms and the propagation velocity about c/4 (c=the speed of light) or 7.5 cm/ns. To operate at a 2 ns data rate, the transit time on the bus should preferably be kept under 1 ns, to leave 1 ns for the setup and hold time of the input receivers (described below) plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm for maximum performance. Lower performance systems may have much longer lines, e.g. a 4 ns bus may have 24 cm lines (3 ns transit time, 1 ns setup and hold time).

US-CL-CURRENT: 327/292

US-PAT-NO: 5578940
DOCUMENT-IDENTIFIER: US 5578940 A
TITLE: Modular **bus** with single or double parallel **termination**
DATE-ISSUED: November 26, 1996
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dillon; John B.	Palo Alto	CA	N/A	N/A
Nimmagadda; Srinivas	Santa Clara	CA	N/A	N/A
Moncayo; Alfredo	Redwood City	CA	N/A	N/A

US-CL-CURRENT: 326/30,327/292
ABSTRACT:

A modular **bus** permitting single or double **termination** is described. The **bus** includes a **terminated** motherboard data net for communicating data signals between a master and one or more motherboard devices. A socket is used for coupling the data signals between the motherboard data net and a terminated module data net of a removable module. The module data net communicates the data signals between the master and one or more module devices. The data signal swing and level of reflection of the data signals are substantially independent of the presence of the module.

18 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

TTL:
Modular **bus** with single or double parallel **termination**

ASNM:
Rambus, Inc.

ABPL:
A modular **bus** permitting single or double **termination** is described. The **bus** includes a **terminated** motherboard data net for communicating data signals between a master and one or more motherboard devices. A socket is used for coupling the data signals between the motherboard data net and a terminated module data net of a removable module. The module data net communicates the data signals between the master and one or more module devices. The data signal swing and level of reflection of the data signals are substantially independent of the presence of the module.

BSPR:
This invention relates to the field of bus architectures. In particular this invention relates to a high speed modular **bus** architecture that converts between single **termination** without a module and double **termination** with a module.

BSPR:
One prior art method of decreasing the effect of reflections requires the use of terminators. A **terminator** is a dissipative load, typically a resistor, located at the end of a transmission **line**. The **terminator** is chosen to have an impedance that matches the characteristic impedance of the transmission **line**. Prior art termination architectures include series termination and parallel

termination.

BSPR:
In series **termination, the terminating** resistor is placed in series with the device driving the transmission **line**. In parallel **termination,** the device drives the transmission **line** directly and a **terminator** is placed at one or both
ends of the transmission **line**. A **bus** with a parallel **termination** at one end of
the **bus** is referred to as a single parallel **termination bus**. Alternatively such a **bus** may be called a singly **terminated bus**. A **bus** with parallel **terminations** at both ends is referred to as a double parallel **termination bus**. Alternatively such a **bus** may be called a doubly **terminated bus**.

BSPR:
In one prior art singly **terminated bus, the terminator** is replaced with an extended **bus** segment containing a **terminator**. The extended bus segment includes the expansion modules. In another prior art singly **terminated bus,** all expansion sockets on the **bus** are populated with either a functional module or a "dummy module". The functional module is a module such as a memory expansion module. The dummy module in this case is a module designed to provide the same effective load as a functional module. Thus in either of these cases the **bus** is always maintained as a singly **terminated bus** either with
or without the modules.

BSPR:
Double parallel **termination** is commonly used in high speed **bus** architectures. In one prior art doubly **terminated bus** architecture, modules are plugged into or removed from a doubly **terminated bus**. The modules effectively tap into the bus. Bus discontinuities will result whenever a tap does not have a module plugged into it. In some cases the modules are inserted or removed regardless of the impedance mismatch. One disadvantage of this technique is the degradation of system performance as described above. Alternatively, the taps can be populated with dummy modules. One disadvantage of this technique is the
complication and cost of additional dummy modules. Thus the **bus** is effectively
maintained as a double parallel **termination bus**. One disadvantage of such a system is that dummy modules must be available to replace the removed modules.

BSPR:
In one prior art doubly **terminated bus,** the modules include **bus** segments that are daisy-chained together as more modules are added to the system. The modules are connected onto a **bus** already having a **terminator**. The last module would have to be a dummy module having a second terminator. This architecture always requires a dummy terminator module as the last module in the chain. In addition to the disadvantage of requiring the dummy module, this architecture requires "shuffling" the dummy module to another location every time the number
of modules on the bus changes.

BSPR:
In view of limitations of known systems and methods, one of the objectives of the present invention is to provide a modular **bus** that permits either single or
double parallel **termination**. The **bus** includes a **terminated** motherboard data net for communicating data signals between a master and one or more

motherboard
devices. A socket is used for coupling the data signals between the motherboard data net and a terminated module data net of a removable module. The module data net communicates the data signals between the master and one or
more module devices. The data signal swing and level of reflection of the data
signals are substantially independent of the presence of the module.

BSPR:
A bus having a clock signal swing substantially independent of the presence of the module is also described. The **bus** includes a **terminated** motherboard clock net for communicating a first clock signal to one or more motherboard devices. A clock signal splitter provides the first clock signal and a second clock signal from a source clock signal. A socket communicates at least one of the first clock signal and the second clock signal to a terminated module clock net
for one or more module devices.

DEPR:
FIG. 1 illustrates the clock and data net topologies for a single channel bus on a motherboard with module 120 plugged in. "Bus" refers collectively to the bus segments coupled to master ASIC 110. In other words, "bus" refers to the motherboard bus and the module bus collectively when the module is plugged in. Without the module "bus" refers only to the motherboard bus. The bus includes module bus 102 and motherboard bus 104. The motherboard **bus** is a singly **terminated bus**. The module **bus is also terminated**. Without the module, the **bus** is a singly **terminated bus**. With the module, the **bus** is a doubly **terminated bus**. The module bus includes module clock net 166 and module data net 172. The motherboard bus 104 includes motherboard clock net 165 and motherboard data net 174.

DEPR:
FIG. 2 illustrates data net 170 modeled as a transmission line. Referring also
to FIG. 1, the portion of the motherboard data net from master ASIC 110 to the socket for inserting the module is modeled as stub 210. A stub is a section of
transmission **line** connected to the main transmission **line** and containing an essentially non-dissipative **termination**. The motherboard data net includes segment 240 attributable to the motherboard slaves and segment 250 from the last motherboard slave to the motherboard data net terminating resistor (192). The module data net includes segment 220 attributable to the module slaves and segment 230 from the last module slave to the module data net terminating resistor (182). Socket 260 couples the module data net to motherboard data net
including stub 210. Terminating resistors 182 and 192 are not shown in this data net model.

CLPR:
3. The **bus** of claim 2 wherein the second clock signal is communicated to a non-**terminated** end of the module clock net, wherein the socket couples a module
clock net transmit node to a motherboard clock net transmit node, the socket couples a module clock net receive node to a motherboard clock net receive node.

CLPR:
6. The **bus** of claim 2 wherein the second clock signal is communicated to a

non-**terminated** end of the module clock net, wherein the first clock signal is not communicated to the module clock net.

CLPR:
9. The **bus** of claim 2 wherein a **terminating** resistance of each of the module clock net, the module data net, the motherboard clock net, and the motherboard data net is in a range of 35 to 55 ohms.

US-CL-CURRENT: 326/30,326/86 ,327/108

US-PAT-NO: 5355391
DOCUMENT-IDENTIFIER: US 5355391 A
TITLE: High speed bus system
DATE-ISSUED: October 11, 1994
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Horowitz; Mark A.	Palo Alto	CA	N/A	N/A
Lee; Winston K. M.	South San Francisco	CA	N/A	N/A

US-CL-CURRENT: 375/257,326/30 ,326/86 ,327/108
ABSTRACT:
In the high speed bus system of the present invention, the bus configuration
is one in which all master devices are clustered at one end of an unterminated end of the bus. The slaves are located along the remaining length of the **bus** and the opposite end of the transmission **line of the bus is terminated**. By eliminating the **termination** resistor at the end of the **bus** where the master devices are located the required drive current needed to produce a given output
swing is reduced. The bus drivers and receivers are CMOS integrated circuits. The bus of the present invention is operable utilizing small swing signals which enable sufficient implementation of current mode drivers for low impedance bus signals. In particular, the bus input receiver of the present invention comprises a two stage buffered sampler/amplifier which receives a small swing signal from the bus and samples and amplifies the low swing signal to a full swing signal within a single clock cycle using CMOS circuits.
23 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

ASNM:
Rambus, Inc.

ABPL:
In the high speed bus system of the present invention, the bus configuration is
one in which all master devices are clustered at one end of an unterminated end
of the bus. The slaves are located along the remaining length of the **bus** and the opposite end of the transmission **line of the bus is terminated**. By eliminating the **termination** resistor at the end of the **bus** where the master devices are located the required drive current needed to produce a given output
swing is reduced. The bus drivers and receivers are CMOS integrated circuits. The bus of the present invention is operable utilizing small swing signals which enable sufficient implementation of current mode drivers for low impedance bus signals. In particular, the bus input receiver of the present invention comprises a two stage buffered sampler/amplifier which receives a small swing signal from the bus and samples and amplifies the low swing signal to a full swing signal within a single clock cycle using CMOS circuits.

BSPR:
Computer buses provide the means for interconnecting a plurality of computer devices such that the devices may communicate with one another. The buses

typically connect master devices such as microprocessors or peripheral controllers and slave devices such as memory components or bus transceivers. Typically the master and slave devices are located at a position along the **bus and the bus is terminated** at both ends of the transmission **line of the bus**. In a doubly **terminated bus,** both ends of the **bus** signal **lines** are connected to **termination** resistors of an impedance which corresponds to the impedance of the signal **lines**. Thus, when a signal is carried along the transmission **line of the bus to the termination** resistor, the resistor absorbs the signal eliminating signal reflections which may occur on the **bus** and cause erroneous signals.

BSPR:
When the **bus** is doubly **terminated,** each driver of a device on a **bus** must effectively drive two **buses** in parallel, one going to the left and one going to the right of the device's location on the **bus**. These signals propagate down the **bus and the bus** will then have been settled when both signals reach the **termination** resistors. The worst case signal settling time for this bus configuration is equal to the time-of-flight delay, t.sub.f, on the bus and which occurs when a driver on one end of the bus is transmitting to a receiver at the opposite end of the bus. The problem with this type of configuration is that the power dissipated by the device driving the bus is quite high since the impedance of the bus is relatively low.

BSPR:
In the high speed bus system of the present invention, the bus configuration is one in which all master devices are clustered at an unterminated end of the bus. The slaves are located along the remaining length of the **bus** and the opposite end of the transmission **line of the bus is terminated**. Elimination of the **termination** resistor at the end of the **bus** where the master devices are located minimizes power dissipation while maintaining the voltage output swing needed to drive the **bus**. The bus drivers and receivers are preferably CMOS integrated circuits. The bus of the present invention is operable utilizing small swing signals which enable efficient implementation of current mode drivers for low impedance bus signals. In particular, the bus input receiver of the present invention receives a small swing signal from the bus and samples and amplifies the small swing signal to a full swing signal within a single clock cycle using CMOS circuits which are buffered to minimize distortion due to back injected signals generated by the sampling process.

DEPR:
The Bus configuration employed in the high speed, low impendance current driven bus of the present invention is illustrated by the block diagram of FIG. 1. Master devices connected to the bus 10, 20 are coupled at one end 25 of the transmission line 5 of the bus. The slave devices 30, 35, 40, 45 are coupled along the transmission line 5. The opposite end 50 of the transmission **line** 5 is **terminated by termination** resistor 55. As noted earlier, the problem with prior art bus configurations is that the power dissipated by the device driving the bus is quite high since the impedance of the bus is relatively low.

DEPR:
In the configuration of the present invention, the amount of power required is reduced by employing this **bus** configuration as the removal of the **termination** resistor at the end 55 of the **bus** reduces the required drive current needed to produce a given output swing. As the master devices are located at the end of the bus, the current driven by the master device output driver produces a full swing signal that propagates along the bus to a slave device. A slave device, located at a point along the bus between the two end points 25, 50 will produce
a drive current that is divided at the output to generate a 1/2 swing signal towards the first end 25 and a 1/2 swing towards the second end 50. By locating the master devices at the end 25 of the **bus** and omitting a **termination**
resistor, the master devices will receive a full swing signal resultant of the sum of the 1/2 swing signal and a 1/2 swing signal which is the reflection of the 1/2 swing signal. Thus the master devices placed within the region where the 1/2 swing signal is doubled will receive a full swing signal due to the sum
of the signal and the reflected signal. Preferably the master devices are located at the point where the signal reflection occurs. However, the extent of the region is dictated by the signal width and the signal propagation time along the bus.

DEPR:
Although the removal of the **termination** resistor at one end causes the **bus** to settle more slowly, this added delay is not a factor since the **bus** transactions
start or end at the master end of the **bus** 25. Removal of the **termination** resistors from one end of the **bus** leaves the worst case delay to be t.sub.f, the same worst case delay found in prior art **bus** configuration.

DEPR:
This delay, t.sub.f, may be better explained by example. In the case of a master device 10 transmitting to a slave device the master sees only a single transmission line of impedance Z as it is connected at the open end of the bus.
If the current source of the driving device has a strength I, a signal voltage of I*Z is transmitted down the bus. The signal arrives at the **termination** resistor and stops at the **termination** resistor 55 so that the **bus** settles after
one time-of-flight delay, t.sub.f. If a signal is transmitted from a slave device to a master device, the device sees two transmission lines, one in either direction, and sends a signal voltage of I*Z/2 in both directions. The signal that travels toward the terminated end reaches the resistor 55 and stops. The signal that travels toward the unterminated end 25 reaches the end 25 and reflects back in the opposite direction doubling in amplitude to provide
the needed swing. However, as the master devices 10, 20 are at that end of the
bus 25, the devices 10, 20 see the final value after only one t.sub.f even though the bus has not yet fully settled.

DEPR:
It should be noted that the reflected signal that travels back down the bus causes inter-symbol interference for the other slave devices on the bus; but this is not important since the slaves only communicate data to the master and not to other slaves. It is important, however, that the reflective wave not encounter any further disturbances which would cause secondary reflections

back
to the master, which may cause interference at the master. A potential source of such disturbances is the original slave transmitter on the bus. In the more
common type of bus transmitter which uses a voltage source, the low impedance driver would cause a secondary reflection which would again reflect off the unterminated end 25 of the bus and would continue until the energy of the wave was dissipated by line losses. Such a situation could result in very long settling times. In the high speed bus of the present invention, current mode sources are used which presents a high impedance to the reflective wave. Thus,
the reflective wave continues to propagate to the **terminated** end of the **bus** where it is absorbed by the **termination** resistor 55.

CLPV:
a **termination** resistor located at the second end of the transmission **line,** said
resistor having an impedance equivalent to the impedance of the transmission **line** whereby signals which travel to the second end of the transmission **line** are absorbed;

CLPV:
said **terminating** resistor absorbing the first 1/2 swing signal, said second 1/2
swing signal reaching the first end of the transmission **line** and reflecting back towards the second end of the **bus,** said master devices located at the first end of the **bus** receiving a full swing signal resulting from the sum of the first 1/2 swing signal and reflected first 1/2 swing signal;

US-PAT-NO: 5319755
DOCUMENT-IDENTIFIER: US 5319755 A
TITLE: Integrated circuit I/O using high performance bus interface
DATE-ISSUED: June 7, 1994
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Farmwald; Michael	Berkeley	CA	N/A	N/A
Horowitz; Mark	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 710/104

ABSTRACT:
An apparatus for storing and retrieving data is described. The apparatus includes a circuitry for initiating data transmission, a first memory, a second memory, and a multiline bus for transferring control information, addresses, and the data. The control information includes information for selecting one of the first and second memories without using any separate memory select line.
Configuration circuitry is provided for assigning a first identification value to the first memory and a second identification value to the second memory. The configuration circuitry includes a first reset line for coupling the circuitry for initiating data transmission to the first memory, a second reset line for coupling the first memory to the second memory, a first identification register for the first memory, a second identification register for the second memory, circuitry for generating a first reset signal and a second reset signal and for sending the first and second reset signals to the first identification register, circuitry for propagating the first and second reset signals from the first identification register to the second identification register, circuitry for resetting the first and second identification registers in response to the first reset signal, and circuitry for setting the first identification register to the first identification value and the second identification register to the second identification value in response to the second reset signal.
59 Claims, 17 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

ASNM:
Rambus, Inc.

BSPR:
High bus bandwidth is achieved by running the bus at a very high clock rate (hundreds of MHz). This high clock rate is made possible by the constrained environment of the bus. The **bus lines** are controlled-impedance, doubly-**terminated lines**. For a data rate of 500 MHz, the maximum bus propagation time is less than 1 ns (the physical bus length is about 10 cm). In addition, because of the packaging used, the pitch of the pins can be very close to the pitch of the pads. The loading on the bus resulting from the individual devices is very small. In a preferred implementation, this generally allows stub capacitances of 1-2 pF and inductances of 0.5-2 nH. Each device 15, 16, 17, shown in FIG. 3, only has pins on one side and these pins connect directly to the bus 18. A transceiver device 19 can be included to interface multiple units to a higher order bus through pins 20.

DEPR:
By using devices with very low power dissipation and close physical packing, the bus can be made quite short, which in turn allows for short propagation times and high data rates. The **bus** of a preferred embodiment of the present invention consists of a set of resistor**-terminated** controlled impedance transmission **lines** which can operate up to a data rate of 500 MHz (2 ns cycles). The characteristics of the transmission lines are strongly affected by the loading caused by the DRAMs (or other slaves) mounted on the bus. These devices add lumped capacitance to the lines which both lowers the impedance of the lines and decreases the transmission speed. In the loaded environment, the bus impedance is likely to be on the order of 25 ohms and the propagation velocity about c/4 (c=the speed of light) or 7.5 cm/ns. To operate at a 2 ns data rate, the transit time on the bus should preferably be kept under 1 ns, to leave 1 ns for the setup and hold time of the input receivers (described below) plus clock skew. Thus the bus lines must be kept quite short, under about 8 cm for maximum performance. Lower performance systems may have much longer lines, e.g. a 4 ns bus may have 24 cm lines (3 ns transit time, 1 ns setup and hold time).

CLPR:
54. The apparatus of claim 53 for storing and retrieving data, wherein each transmission **line is terminated**.

US-CL-CURRENT: 326/86,327/541

US-PAT-NO: 5254883
DOCUMENT-IDENTIFIER: US 5254883 A
TITLE: Electrical current source circuitry for a bus
DATE-ISSUED: October 19, 1993
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Horowitz; Mark A.	Palo Alto	CA	N/A	N/A
Gasbarro; James A.	Mountain View	CA	N/A	N/A
Leung; Wingyu	Cupertino	CA	N/A	N/A

US-CL-CURRENT: 326/30,326/86 ,327/541
ABSTRACT:

Electrical current source circuitry for a bus is described. The circuitry includes transistor circuitry coupled between the bus and ground for controlling bus current, control circuitry coupled to the transistor circuitry,
and a controller coupled to the control circuitry for controlling the transistor circuitry. The controller comprises a variable level circuit comprising setting circuitry for setting a desired current for the bus and transistor reference circuitry coupled to the setting circuitry. The variable level circuit provides a first voltage. Voltage reference circuitry provides a
reference voltage. Comparison circuitry is coupled to the voltage reference circuitry and to the variable level circuit for comparing the first voltage with the reference voltage.. Logic circuitry is responsive to a trigger signal from the comparison circuitry. An output of the logic circuitry is coupled to the control circuitry in order to turn on the transistor circuitry in a manner dependent upon an output of the logic circuitry.
39 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

ASNM:
Rambus, Inc.

DEPR:
Data transmission lines 32 comprise nine transmission lines. These transmission lines are matched transmission lines and have controlled impedances. Each **line** of data transmission **lines** 32 is **terminated** at one end by a **termination** resistor. As shown in FIG. 1, there are nine **termination** resistors, each connected to a respective one of data transmission **lines** 32. These termination resistors are collectively referred to as termination resistors 20. Termination resistors 20 are coupled to termination voltage V.sub.term.

DEPR:
The resistance value of each of **termination** resistors 20 is R, which is equal to the **line** impedance of each transmission **line** of data transmission **lines** 32. In one embodiment, the termination voltage V.sub.term is approximately 2.5 volts. Each of the **termination** resistors 20 is matched to the respective transmission **line** impedance. This helps to prevent reflections.

DEPR:
BusCtrl line 14 transfers the bus control signal among master 11 and slaves 12a-12n. BusEnable line 15 transfers the bus enable signal among master 11

and
slaves 12a-12n. BusCtrl **line** 14 is **terminated** at one end by **termination** resistor 23. BusEnable **line** 15 is **terminated** at one end by **termination** resistor 21. Termination resistors 21 and 23 are each coupled to the termination voltage V.sub.term. Each of the **termination** resistors 21 and 23 is
matched to the respective **line** impedance. This helps to prevent reflections.

DEPR:
Bus system 10 also includes daisy chain line 13 and clock line 16. Daisy chain
line 13 couples the SOut pin of one device to the SIn pin of another device (i.e., chained) for transferring TTL signals for device initialization. **Line** 16 is **terminated by termination** resistor 22.

DEPR:
In an alternative embodiment, **bus** system 10 may include two masters coupled to the end of **bus** 30 that is opposite **termination** resistors 20, 21, and 23.

DEPR:
Even though the drivers for bus 30 are current mode drivers, bus 30 carries low
voltage swing signals. The current mode drivers of master 11 and slaves 12a-12n control the voltage levels of bus 30. When a current mode driver is in
an "off" state, the respective bus line either stays at or rises to a high voltage level. When the current mode driver is in an "off" state, there is approximately zero voltage drop across the respective termination resistor of resistors 20 because the current mode driver is not providing a path to ground for current. The high voltage level for **bus** 30 is the **termination** voltage V.sub.term.

DEPR:
When a current mode driver is in an "on" state, the current mode driver provides a path to ground for current for the respective bus line. In other words, when the current mode driver is in an "on" state, pull down current flows through the current driver. The low voltage level of bus 30, is accordingly, determined by the pull down current. The pull down current flows through the respective resistor of termination resistor of resistors 20. A voltage drop appears across the respective **termination** resistors 20, and a low voltage level appears on the respective **line of bus** 30. The pull down current (flowing through the output driver and the respective termination resistor) is referred to as the desired current. The magnitude of the desired current can be set or selected by the user to allow for different bus impedance, noise immunity, and power dissipation requirements. Circuitry described below permits the desired current to be substantially independent of processing variations, power supply variations, and temperature variations.

DEPR:
In FIG. 4, driver 100 is coupled to data transmission line 111 via output pad 110. Data transmission line 111 is one of the data transmission lines 32 of bus 30. Transmission **line** 111 is coupled to the **termination** voltage V.sub.term
via **termination** resistor 112 that resides at one end. Termination resistor 112
is one of resistors 20.

DEPR:

Transistors 101a-101e are used to provide a path to ground for current. When one or more of transistors 101a-101e is turned on, current flows through each transistor that is turned on. The current flow results in a voltage drop across resistor 112. This results in the lowering of the voltage on line 111 of bus 30. When transistors 101a-101e are all turned off, then no current flows through transistors 101. This means that no current flows through resistor 112, so there is no voltage drop across resistor 112. Thus, when transistors 101a-101e are all turned off, the **termination** voltage V.sub.term appears on **line** 111 of **bus** 30. Thus, transistors 101 are used to control current and voltage with respect to line 111 of bus 30. Turning on various combinations of transistors 101a-101e results in various currents and voltages with respect to line 111 of bus 30.

DEPR:
Because of the 10:1 scaling of the widths of transistors 101a-101e (of FIG. 4) with respect to transistors 127a-127e and because of the 5:1 scaling of resistors 31 and 112, the count of counter 133 represents the value that can turn on the same combination of transistors 101a-101e to provide the desired current I on transmission line 111. The desired current I results in a V.sub.OL voltage on transmission **line** 111 given the current flow through **termination** resistor 112.

DEPR:
When the data applied to transistor 222 is a logical high signal, transistor 222 is turned on. Resistor 230 is a relatively small resistance. Therefore, when transistor 222 is turned on, the emitter of transistor 224 sees a voltage that is greater than the termination voltage. Therefore, transistor 224 does not conduct current. Therefore, current does not flow through line 111. Accordingly, a high voltage equal to the **termination** voltage appears on **line** 111.

DEPR:
During operation, when the data applied to the gate of transistor 258 is logically high, transistor 258 is turned on. This causes the gate of transistor 254 to be shorted to ground, which turns transistor 254 off. When transistor 254 is off, no current flows through transmission line 111. Therefore, the **termination** voltage appears on **line** 111.

CLPR:
15. An output driver for an electronic device coupled to a **bus, wherein the bus** is coupled to a voltage supply via a **termination** resistor, wherein the output driver comprises:

CLPR:
26. An output driver for an electronic device coupled to a **bus, wherein the bus** is coupled to a voltage supply via a **termination** resistor, wherein the output driver comprises: